TABLE OF CONTENTS

DISCLAIMER

Intercontinental Micro Systems Corp. makes no representations or warranties with respect to the contents hereof and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Intercontinental Micro Systems Corp. reserves the right to revise this publication and to make changes from time to time in the content hereof without obligation of Intercontinental Micro Systems Corp. to notify any person of such revision or changes.

**** INTRODUCTION ****

The INTERCONTINENTAL MICRO SYSTEMS CORP. (ICM) CPZ-48000 single board central processor is a Z80A (tm) based computer board designed to meet or exceed the IEEE S-100 Bus specification. This third generation computer incorporates all the features necessary for a complete, stand alone CP/M (tm) system and is perfect for use in multi-processor or multi-user/multi-tasking architectures utilizing operating systems such as MP/M (tm), OASIS (tm), TURBODOS (tm) and CP/NET (tm).

Features such as an independent interrupt structure, Direct Memory Access, a 16 Megabyte Memory Management Unit and a bank selectable on-board 64K memory coupled with I/O devices such as a floppy disk controller, a 2-port serial controller and a 2-port parallel controller provides the user computing power on a single board heretofore unmatched in the S-100 Bus industry. Other features incorporated are listed as follows:

FEATURES

* IEEE S-100 Bus Compliance
* Z80A (tm) 4MHz Operation
* Single or Double Density Floppy Disk controller with up to four 8" or 5 1/4" floppy disk drives in either DMA, Interrupt or Programmed I/O mode.
* Two Serial I/O channels with one channel programmable in either DMA, Interrupt or Programmed I/O mode.
* Two Parallel I/O channels with one channel programmable in either DMA, Interrupt or Programmed I/O mode.
* Four Channel Direct Memory Access Controller
* 64 Kbytes of On-Board Dynamic RAM with Memory Deselect of 4 Kbytes to 64 Kbytes under software control
* Memory Management of 16 Megabytes of system memory
* Eight Vectored Priority Interrupts chained together with I/O Interrupts for use with Z-80 Mode 2 Interrupts
* Provisions for either a 2 Kbyte or 4 Kbyte on-board EPROM (Monitor in a 2 Kbyte EPROM supplied with board.)
* Software Selectable Baud Rates
* Real Time Clock
* Synchronous or Asynchronous operation using the Z80A SIO chip
* CP/M (tm) and MP/M (tm) Operating Systems available
* Turbo-Disk (tm) Implementation Included

PERFORMANCE SPECIFICATIONS

MICROPROCESSOR
- Clock rate.....4MHz
- Type.....Z80A

BUS INTERFACE.....IEEE S-100

SERIAL I/O CHANNELS
- Synchronous Operation
  - Baud Rate.....Up to 800K Baud
  - Data Transfer.....DMA, Interrupt or Programmed I/O
- Asynchronous Operation
  - Baud Rate.....Up to 50K Baud
  - Clock Rate.....1, 16, 32 or 64 Times Baud Rate
  - Bits/Character.....5, 6, 7 or 8
  - Stop Bits..... 1, 1 1/2 or 2
  - Parity.....Odd, Even or None
  - Data Transfer.....DMA, Interrupt or Programmed I/O
  - I/O Interface.....Through Personality Boards

PARALLEL I/O CHANNELS
- Data Rate.....Up to 300K Bytes/Sec
- Channel A Data Transfer.....DMA, Interrupt or Programmed I/O
- Channel B Data Transfer.....Interrupt or Programmed I/O
- Interface Signals.....16 Data Lines Plus 4 Handshaking Lines
- I/O Interface.....Through Personality Boards

FLOPPY DISK CONTROLLER
- Data Rate/8-Inch Double-Density.....500,000 Bits/Sec
- Data Rate/8-Inch Single-Density.....250,000 Bits/Sec
- Data Rate/5 1/4-Inch Double-Density.....250,000 Bits/Sec
- Data Rate/5 1/4-Inch Single-Density.....125,000 Bits/Sec
- Format.....IBM 3740 or 512 sectors
- Data Transfer.....DMA, Interrupt or Programmed I/O
- I/O Interface.....Through Personality Boards

INTERRUPT CONTROL
- Number of Channels.....8
- Priority.....Rotating or Fixed
- Interrupt Modes.....Z80 Mode 0, Mode 1 or Mode 2

REAL-TIME CLOCK
- Operation.....Software Polled or Interrupt Driven
- Range.....37.5 Hz to 1.2288 MHz

64K DYNAMIC RAM MEMORY

Bank Selection.....May be bank selected in increments of 4K to 64K commencing at 4K boundaries; e.g. 8K of memory may be selected or deselected commencing at location COOO(hex) as defined by software.

Wait States.....None

Direct Memory Transfers.....To/From SIO, PIO or FDC

DIRECT MEMORY ACCESS CONTROLLER

Channel 0.....Cascade Mode for IEEE S-100 Bus or Used with Channel 1 in Memory-to-Memory Transfers

Channel 1.....Channel A of SIO Controller

Channel 2.....Floppy Disk Controller

Channel 3.....Channel A of PIO Controller

EPROM

Type.....2716 2K EPROM or 2732 4K EPROM

Wait States.....None

Functions.....Bootup and Monitor

POWER REQUIREMENTS

Voltages.....+8 VDC @ 2.5 A (max)
+16 VDC @ 0.2 A (max)
-16 VDC @ 0.2 A (max)

Power.....22 W (max)

OPERATING ENVIRONMENT

Temperature.....0 to 45 Degrees Celsius

Relative Humidity.....0 to 95%

CONSTRUCTION

Circuit Board.....Four Layer Glass Epoxy, Soldermask over Copper. All IC's in Sockets

Connectors.....Shrouded for Protection

TESTING.....Tested and Burned-In

WARRANTY.....Full One Year Warranty (Parts and Labor)

* Z80 is a Trademark of Zilog, Inc.
CP/M, MP/M and CP/NET are Trademarks of Digital Research
OASIS is a Trademark of Phase One Systems
TURBODOS is a Trademark of Software 2000, Inc.

**** FUNCTIONAL DESCRIPTION ****

The CPZ-48000 is functionally partitioned into the following major groups:

- INPUT/OUTPUT STRUCTURE
  - OFF-BOARD PERIPHERAL CONTROLLERS
    - SERIAL I/O PORT CONTROL
    - PARALLEL I/O PORT CONTROL
    - FLOPPY DISK CONTROL
  - ON-BOARD PERIPHERAL CONTROLLERS
    - DMA CONTROL
    - INTERRUPT CONTROL
    - MEMORY MANAGEMENT UNIT
- 64 KBYTE DYNAMIC RAM/LOGIC
- 2/4 KBYTE EPROM
- INPUT/OUTPUT CHIP SELECT LOGIC
- CPU CONTROL SIGNALS GENERATOR
- CLOCK GENERATOR
- POWER-ON CLEAR/RESET LOGIC
- S-100 BUS INTERFACE

Each group is described below to give the user a clear understanding of the hardware and software setup options and to give a full appreciation of the computing power available to the user.

INPUT/OUTPUT STRUCTURE

As a point of reference, an I/O device is defined as a device which, under program control of the Z80 CPU, controls a peripheral device or memory.

The I/O devices contained on the CPZ-48000 consist of:

- Z80A SIO-0 (Serial Port Controller, SIO)
- Z80A PIO (Parallel Port Controller, PIO)
- WD1793 + SUPPORT CHIPS (Floppy Disk Controller, FDC)
- AM 9517A-4 (Direct Memory Access Controller, DMA)
- AM 9519A (Universal Interrupt Controller, UIC)
- 8253 (Programmable Timer/Counter, PTC)
- 74LS610 (Memory Management Unit, MMU)

Of these, the first three are used to communicate with off-board peripheral devices and will be referred to as the "OFF-BOARD" peripheral I/O controllers. The remaining are "ON-BOARD" I/O controllers.

Programmed I/O, Interrupt or Direct Memory Access (DMA) is possible to/from SIO port A, PIO port A and the FDC. No DMA is possible for SIO port B or PIO port B. A DMA port is assigned to the S-100 Bus DMA request line to allow temporary bus masters to capture the bus for DMA transfers to off-board memory. Either fixed or rotating priority selection allows arbitration between internal DMA and external DMA requests from the S-100 Bus. Selection of fixed priority gives the S-100 Bus the highest priority and PIO port A, the lowest. Thus,

DEVICE	PRIORITY
S-100 Bus	1 High
SIO A	2
FDC	3
PIO A	4 Low

The CPZ-48000 uses 128 of it's possible 256 I/O port address for on-board use. The range used is from 80 Hex to FF Hex. Please refer to the SOFTWARE Section of this manual for further explanation.

OFF-BOARD I/O CONTROLLERS

The Off-Board I/O Controllers consist of the Serial I/O Port Control, Parallel I/O Port Control and the Floppy Disk Control.

SERIAL I/O PORT CONTROL

The Serial I/O Port Control consists of the Serial I/O Controller and the Baud Rate Clock Generator.

Serial I/O Controller

The Serial I/O (SIO) Controller is a programmable dual channel device which provides formatting for serial data communications. The channels can handle either asynchronous or synchronous data transfers to/from serial peripheral devices. The SIO operates either under programmed I/O, Interrupt Control or DMA control. DMA is provided for Port A only. All lines necessary to handle asynchronous, synchronous, synchronous bit oriented protocols and other serial protocols are available to the user at the interface connectors. In addition, +/- 16 volt DC and +5 volt DC power are available at these connectors.

The SIO may be interfaced to peripheral devices requiring differing protocols. This interface is tailored to the exact device requirements by use of a Personality Module. The interface is implemented through two 16-pin Ansley connectors. Refer to Appendix A for a description of the serial Personality Modules currently available.

To program the SIO, the system software issues commands to initiate the mode of operation. Seven write registers exist for that purpose. In addition, three read registers allow the programmer to read the status of each channel.

Baud Rate Clock Generator

The Baud Rate Clock Generator consists of a clock generator and an 8253 Programmable Interval Timer. The 8253 is a device which, under software control, can generate variable clock periods which are a multiple of the base input clock. The device has other modes of operation; however, only the mode applicable to the CPZ-48000 operation will be described here. This is Mode 3, the square wave generator mode.

The 8253 consists of three channels, each with a clock input and a gate input. Channel 0 is tied to SIO channel A transmit and receiver clock inputs, channel 1 to SIO Channel B transmit and receiver clock inputs, and channel 2 to the interrupt select jumper area (as a select input to the 9519A Interrupt Controller). Channels 0 and 1 are intended for baud rate clocks, whereas channel 2 is intended for the "real time" clock.

Channels 0 and 1 are connected to the SIO inputs via jumper options PJB and PJA. These signals are also tied to the serial interface connectors. If clock signals are originated by the interfacing devices, the jumpers are cut appropriately. The channel A jumper provides for separate transmit and receive clock inputs from the interface (connector J2) or may serve as baud rate generator outputs to the interface. This arrangement is intended to provide a clock to synchronous MODEM's via "external" clock (pin 24 of the S-100 Bus) in accordance with the EIA RS-232C standards. The modem can then return a transmit/receive clock to the serial controller. In summary, means are provided to implement serial interfaces accommodating asynchronous, synchronous, HDLC and a great number of currently defined communications protocols.

While operating in Mode 3, the 8253 generates a square wave whose period is defined by a count programmed into the respective channel's counter. The square wave will remain at a logical ZERO

state for one half the count, and at logical ONE for the remaining half of the count. The counter decrements for each clock period that is received.

The 8253 is programmed by the CPU specifying the mode, loading sequence and counter contents. The Baud rates that can be derived from the 2.4576 Megahertz clock are listed as follows:

Baud Rate	Theoretical Frequency (16 x clock)
50	0.8 kiloHertz
75	1.2 kiloHertz
110	1.76 kiloHertz
134.5	2.152 kiloHertz
150	2.4 kiloHertz
300	4.8 kiloHertz
600	9.6 kiloHertz
1200	19.2 kiloHertz
1800	28.8 kiloHertz
2000	32.0 kiloHertz
2400	38.4 kiloHertz
3600	57.6 kiloHertz
4800	76.8 kiloHertz
7200	115.2 kiloHertz
9600	153.6 kiloHertz
19200	307.2 kiloHertz

PARALLEL I/O PORT CONTROL INTERFACE

The parallel I/O Port Control Interface consists of the Parallel I/O Controller (PIO). The Parallel I/O Controller is a programmable two-port LSI component, which interfaces peripheral devices to the Z80 microprocessor. The PIO provides data transfer to and from peripheral devices under programmed I/O, interrupt control or DMA control. Handshaking data transfer control lines are provided to the interface in addition to the two eight-bit data ports. The CPU reset line and the CPU clock are also connected to this interface. The PIO is flexible and may be connected to peripheral devices requiring differing protocols.

The interface is tailored to the exact device requirements by use of a "Personality Module". The Personality Module is a small external circuit board which connects to the CPZ-48000 to provide the hardware drivers and receivers, logic and other circuitry as required. Refer to Appendix A for a description of the parallel Personality Modules currently available.

An interrupt line is brought into the interface to give the user the capability of servicing interrupts. The interface is implemented through a 26-pin Ansley connector.

To program the PIO, the system software issues commands to initialize the mode of operation. Initialization is provided by loading the interrupt vector, mode, I/O and interrupt control registers.

Double- or Single-Density Floppy Disk Controller (FDC)

The CPZ-48000 uses the Western Digital WD1793 or the Fujitsu MB8877 Floppy Disk Controller plus the WD2143 and WD1691 support chips as the basis for the controller. A reliable phase-lock-loop circuit is implemented giving the user error free disk operation. Up to four 8-inch or 5 1/4-inch Floppy Disk drives may be connected. A mix of single- or double-sided drives and of single- or double-density drives may be interconnected. The only limitation is that 8" and 5 1/4" drives cannot be mixed. Any combination of single/double sided and single/double density drives may be connected.

The FDC is connected to the drives via a Personality board FPB100-XY and an adaptor board depending on the type of drive (8" or 5 1/4") and type of cable. For example, an FPB100-11 consists of the personality board and an edge card connector adapter for 5 1/4-inch Floppy drives. Header plug connector adaptors are also available.

A jumper option on the FPB100-XY allows the user to configure the board for either 8-inch or 5 1/4-inch. This technique greatly reduces the overall cost of interfacing to floppy drives. With a low cost personality board and even lower cost adaptor, the user may connect the drive configuration fitting his particular needs.

ON-BOARD I/O CONTROLLERS

The On-Board I/O controllers consist of the DMA Controller, Interrupt Control Logic and the Memory Management Unit.

DMA Controller

The DMA Controller consists of the 9517A-4 Multimode DMA Controller, which is a LSI component designed to allow external peripheral devices to transfer data directly to and from the on-board

system memory. The use of this data transfer technique greatly enhances the system data throughput because the Z80 microprocessor does not have to deal directly with the transfers, and is free to perform other computing functions.

DMA Operations

The 9517A is a programmable device, which enables the programmer to free the CPU from the repetitive task of controlling data block transfers by providing "external" hardware control over such operations. For example, the programmer may specify that a data block of "X" number of bytes contained in system memory starting at location "Y" is to be transferred. The programmer may further specify that at the end of said transfer an interrupt is to be generated (perhaps to initiate a subsequent transfer, or to determine the peripheral device status prior to initiating a subsequent transfer). Alternately, the programmer may wish to automatically re-initialize the data block transfer. Once the software command is transmitted to the 9517A, it performs all of the indicated actions without further supervision from the Z80 microprocessor. In all cases, the user of the CPZ-48000 has full control over these parameters and events by having the capability to access any of 27 data and control registers. Once the DMA transfer has begun (also enabled under software control), the CPU may then be used for other processing or for controlling other peripheral data transfers in a similar manner.

The DMA Controller may be operated in either burst or cycle-stealing mode. Cycle-stealing is recommended if concurrent CPU processing is desired while I/O processing is taking place. Burst mode is recommended for operating with fast peripheral devices which could lose data if not responded to in a timely fashion. The transfer rate is 1 megabyte/sec. with DMA operating in burst mode.

DMA Channel Assignments

The CPZ-48000 utilizes all four channels of the 9517A. Channel 0 is dedicated to the S-100 Bus pHOLD line, channel 1 to the SIO serial data channel A, channel 2 to the FDC Data Request Line, and channel 3 to channel A of the PIO parallel I/O port. The DMA channels may be programmed for either fixed or rotating service priority. Selection of fixed priority gives the S-100 Bus the highest priority and parallel port A the lowest. The peripheral device which has higher throughput and which may require closer supervision could connect via the S-100 Bus, or reside in the peripheral device enclosure and communicate via data ports. Should that peripheral be

connected directly to the S-100 Bus, fixed priority servicing is recommended. A memory-to-memory block transfer feature is provided which enables the user to transfer blocks of data from a source area of memory to a destination area of memory with an overall throughput increase of 3 times that available using Z80A block moves. Further, programming overhead is reduced in that the CPU need only initiate the DMA device and enable the DMA transfer. The CPU may then execute other code if so desired.

Combining DMA with the Memory Management Unit (MMU), a block of memory may be transferred from the on board system memory to off-board system memory and vice-versa at DMA Speeds. The MMU is loaded with appropriate address translation information. When the DMA transfers data to addresses translated by the MMU, the data is directed to the off-board memory. Memory-to-memory transfers within the on-board memory may also be made. While the Z80 executes block move transfers (LDIR etc...) at 21 clock cycles per byte, the memory-to-memory function of the DMA controller will move a byte in 7 clock cycles, or 3 times faster.

The S-100 Bus channel (channel 0) is normally operated in "CASCADE" mode. Under cascade mode, the DMA Controller simply isolates the CPZ-48000 from the S-100 Bus while the off-board DMA transfer occurs. The power of this technique is that any number of DMA type devices may reside on the S-100 Bus limited only by system data throughput considerations.

During power-up or reset, the DMA Controller is cleared to a state in which DMA requests registers are masked. The cascade mode and other registers must be programmed before channel 0 is active. This should be done as part of an initialize sequence.

Interrupt Control Logic

The interrupt control logic gives the CPZ-48000 user the power to respond to the maskable interrupt (INT*) in any of three modes. These are referred to as modes 0, 1 and 2. Mode 0 is identical to the 8080 interrupt response mode, whereby the interrupt controller instead of memory can place a restart instruction on the data bus and the CPU will execute it. Mode 1 response is identical to that of a non maskable interrupt, except that a restart to location 0038H is executed instead of to 0066H. Mode 2 response allows the user an indirect call to any memory location within a 64 kilobyte memory address space by forming a 16-bit pointer to a table of interrupt service pointers. The 16-bit address is formed by combining the upper 8-bits of register I of the CPU chip with the lower 8-bits of the interrupting device address to form a pointer to a table of 16-bit

address pointers to the interrupt service routine.

Interrupt Controller/Select

The CPZ-48000 interrupt controller consists of the 9519A Universal Interrupt Controller. This is a LSI device which provides up to eight maskable interrupt request inputs. Upon receipt of an unmasked interrupt request, a byte of previously stored information is output to the data bus. This enables the CPU to process interrupt service routines by executing restarts or indirect jumps to those service routines. Expansion to the interrupt structure is provided by a priority technique in which enable in/enable out signals are connected in series ("daisy- chained"). The higher priority interrupting device's enable input is set to logical ONE by permanently connecting it to a pull-up resistor. The SIO enable input line is pulled up to a logical ONE, its enable output line is tied to the enable input line of the PIO and the PIO enable output line is tied to the enable input line of the 9519A. The enable output line of the 9519A is tied to an S-100 Bus. The eight interrupting channels are serviced on a fixed or rotating basis. Within the SIO, priority is fixed, Channel A is assigned a higher priority than Channel B. The receiver, transmitter, and external status are assigned priority in that order within each channel. Similarly, interrupt priority for the PIO is fixed, with Port A having higher priority than Port B. In summary, the CPZ-48000 interrupt priority daisy chain is as follows:

Priority	Device
1	SIO channel A receiver
2	SIO channel A transmitter
3	SIO channel A external status
4	SIO channel B receiver
5	SIO channel B transmitter
6	SIO channel B external status
7	PIO port A
8	PIO port B
9-16	9519A inputs (fixed or rotating)
17-nn	S-100 Bus interrupt device(s)

NOTE: Any I/O device in the S-100 Bus which uses the INT* line must use this priority chain scheme and must supply its vector. The I/O device must connect to IPROCESS* (response in progress line, pin 65 of the S-100 Bus) and to the PCHAIN (Priority enable output Line, pin 21 of the S-100 Bus). The IPROCESS* connection must be made with an open-collector driver. If the I/O device does not meet these conditions, then it must use the vectored interrupt facility of the S-100 Bus (lines V10*-V17*).

An additional feature of the CPZ-48000 is that data transfers from the peripheral devices may be handled in a polled mode. This requires that the 9519A device be programmed for polled mode and the status register interrogated for the occurrence of the interrupt source signal. In polled mode no interrupts are generated, but the status signal indicating the occurrence of an event remains active. Having detected that occurrence, the remaining status is then interrogated to determine which of the eight events occurred.

Jumper options allow the user to choose among twelve S-100 Bus interrupt signals (VI0* to V17*, INT*, PWRFAIL*, NMI* and ERROR*), as well as six internally generated interrupt signals corresponding to the completion of each of the three DMA transfers, FDC interrupt, the parallel port interrupt, and the real time clock. The user selects eight of these signals to be inputs to the Interrupt Controller. The real time clock allows interrupts to be generated at a programmable rate, or they may be software polled.

Signal	Source
VI0*-V17*	S-100 Bus
FINT*	FDC Interrupt
EDMA1*	SIO channel A DMA end of transfer
EDMA2*	FDC DMA end of transfer
EDMA3*	PIO port A DMA end of transfer
SERR*	S-100 BUS ERROR
RTCLK	Real time clock
PINT*	Parallel port interrupt

The S-100 Bus signal INT* is connected to the CPU's INT* bus via an open-collector gate to OR-tie onto the bus to which the on- board interrupt devices are connected (SIO, PIO and 9519A).

The CPU's non-maskable interrupt line (NMI*) may be selected to respond to signals on the S-100 Bus NMI* or PWRFAIL* line. All of these options are implemented by use of jumper plugs.

MEMORY MANAGEMENT UNIT

The Memory Management Unit consists of the 74LS610 MEMORY MAPPING DEVICE plus associated logic. The 74LS610 is a paged memory mapping device which expands the Z80 16-bit address to 24 bits, increasing the addressing capability of the Z80 from 64K bytes to 16 Megabytes. Two modes of operation are possible. These are the "PASS" and "MAP" modes. The 4 MSBits of the Z80 are input to the 74LS610. These bits address one of sixteen 12-bit registers, the outputs of

which are output on the address bus. In pass mode, the Z80's 4 MSBits merely pass through the 74LS610 to the corresponding 74LS610 address outputs. The remaining 8 bits of extended address lines are forced to logic zero. In map mode, the contents of the addressed mapping register are output on the address bus. This technique proves to be quite powerful since the extended address lines appear on the bus dynamically. The 12 bits of extended address constitute a "PAGE" address. The remaining 12 lower order address lines address the locations within each page. A "PAGE" consists of 4 Kbytes. There are two hundred and fifty-six 4K pages to give a total of 16 megabytes of storage.

The Memory Management Unit allows the user to map any logical 4K block of memory to any physical 4K block within the 16 megabyte range. Thus, several programs or "TASKS". can share one main program by changing logical 4K block addresses.

The Memory Management Unit lends itself to the generation of address lines in compliance with the IEEE S-100 Bus specification. The signal PSTVAL* is input to the 74LS610 to control the transparent latch function. Thus, the address lines as sampled on the falling edge of PSTVAL* are latched for the duration of a memory cycle as required by the specification. The latching operation functions in both the pass and map mode.

64 Kbyte Dynamic RAM/Logic

The 64 Kbyte Dynamic RAM and associated logic consist of eight 64K-by-one-bit Dynamic RAM's, an address multiplexer, RAS/CAS/REFRESH generator, RAM enable logic and the Window Deselect circuitry.

The 64 Kbyte RAM's utilize on-chip auto-refresh logic. This, coupled with additional external logic provides effective refresh techniques suitable for Z80 and S-100 Bus operations. Two octal drivers are utilized to multiplex the 16-bit address lines to the RAM's. A RAS/CAS/REFRESH circuit generates the required timing for the proper reading, writing and refresh operations of the RAM. The RAM enable logic disables the on-board 64 Kbyte RAM when off-board RAM is addressed. The S-100 Bus signal PHANTOM is also sensed to disable the on-board RAM when this signal is active. A Window Deselect Circuitry is provided to perform two functions. The first function is to deselect a portion of RAM during cold-start boot-up to allow a 2 or 4 Kbyte monitor/boot-up PROM to exist in the 64 Kbyte address space without bus conflicts with the RAM. The cold-start boot-up process consists of:

- Deselecting the 1st 4 kbyte locations of the RAM address

space.
- Deselecting all of RAM through commands from the EPROM.
- Relocating the EPROM address to the upper 8K locations of the address space through commands from the EPROM.
- Re-enabling all of RAM except the area in which the EPROM exists (E000-EFFF).
- Performing the Operating System load process.
- At completion of the Operating System load process, deselecting the EPROM through commands loaded in the RAM & enabling all of RAM.

The second function is to deselect a "Window" of RAM as specified under software commands. This "Window" is defined as a section of memory which is enabled or disabled under software control. The window boundaries are specified by the contents of two four-bit registers. One register holds the lower boundary and the other holds the upper boundary. The values of the register can take on any value from 0(hex) to F(hex). In this manner, any window commencing and ending at any 4 Kbyte boundary may be specified. This feature enables the user to configure multi-user bank select architectures using bank selectable memory boards installed in the S-100 Bus. The feature also enables the user to configure systems where an external memory, such as a memory mapped video board, is required to co-exist in the 64 Kbyte address space with the on-board RAM.

2K/4K EPROM

The CPZ-48000 may accommodate either a 2K (2716) or 4K (2732) EPROM. A jumper (jumper JB) is made available to select either of the two EPROM types. The EPROM functions as both a boot-up and a monitor PROM. As a boot-up PROM, the EPROM contains the software routines necessary to manipulate the Window Deselect Circuitry and to load the required Disk Operating System contained on Floppy Disk Drive diskettes. The EPROM also contains monitor routines which are discussed in the SOFTWARE/PROM MONITOR sections.

I/O Chip Select Logic

The I/O Chip Select logic generates the "chip select" signals for the SIO, PIO, programmable counter, universal interrupt controller, FDC, Memory Management Unit (MMU), Boot/Monitor Enable, Memory Deselect Logic, FDC Configuration register and the DMA Controller. In addition, the required control and data signals are generated for the SIO, FDC and PIO. Because the SIO, FDC and PIO may be operated under DMA control (as well as programmed I/O), the chip

select, control and data signals are generated to handle each case within this logic.

POWER-ON CLEAR/RESET LOGIC

This logic provides reset signals to the CPU as well as to the S-100 Bus interface. The logic is activated under two conditions, when power is first applied to the board, and when the S-100 Bus signal RESET* is activated.

Signals asserted upon applying power are:

a. S-100 Bus signals POC*, RESET*, and SLAVE CLR*
b. Internal CPZ-48000 reset

Signals assered when RESET* is asserted are:

a. S-100 Bus signal SLAVE CLR*
b. Internal CPZ-48000 reset

CLOCK GENERATOR

The clock generator divides an eight-Megahertz crystal-generated clock signal to provide the internal CPU clock (0CLK), the S-100 Bus clocks (0 and CLOCK) and internal clocks BUSCLK and SCLK. These clock signals are utilized to implement S-100 Bus signals in conformance with the IEEE standard for the S-100 Bus on a well-defined, clocked-logic basis.

CPU Control Signals Generator

The CPZ-48000 architecture is enhanced by use of state-of-the-art LSI components. The board utilizes a mix of Z80 support components (SIO and PIO) and 8080 support devices (8253, 9519A and 9517A). A variety of logical conflicts arise due to the differing requirements of these components and those of the S-100 control bus. Further, the control signals generated by the DMA Controller differ from Z80-type control signals. It is the function of the CONTROL SIGNALS GENERATOR to generate all of the appropriate control signals required by each of these components and the S-100 BUS CONTROL SIGNALS GENERATOR (described below).

S-100 BUS CONTROL SIGNALS GENERATOR

The S-100 Bus Control Signals Generator consists of the logic necessary to generate key S-100 Bus signals such as pSYNC, pSTVAL*, pWR*, and pDBIN.

pSTVAL* is of particular importance, as this signal is used to to perform a transparent latch function for other signals, the result of which is to generate S-100 Bus signals in conformance with the IEEE timing standards. Address and data lines are latched with this signal whereby status is latched or unlatched as selected by a jumper. While in the latched mode, the CPZ-48000 is set for full IEEE timing conformance. The transparent mode enables systems to operate in conformance with Z80 timing.

Jumper option JC is provided to configure pDBIN to any given system which may not tolerate the stringent IEEE timing requirements for this signal. Read access time can be adjusted by selecting one of the two positions on the header.

S-100 Bus Interface

The S-100 Bus consists of 100 electrical signal lines. These are grouped into sets of lines used to transmit data and control among interconnected devices. The groups are:

Group	No. of Lines
Address Bus	24
Input Data Bus	8
Output Data Bus	8
Status Bus	8
Control Input Bus	5
Control Output Bus	6
DMA Control Bus	8
Vectored Interrupt Bus	8
Utility Bus	8
System Power	9
Manufacturer specified lines	3
Reserved lines	5

Devices connected on the bus are classified as either bus masters or bus slaves and as either permanent or temporary masters. The CPZ-48000 is a permanent bus master. Any other master connected to the S-100 bus may take control of the bus by making the appropriate

DMA request provided no internal DMA by the SIO, FDC, or PIO is in progress. If the DMA controller is programmed for fixed priority operation then the S-100 Bus DMA request will be honored first if simultaneous DMA requests occur.

Each of the S-100 Bus signals utilized by the CPZ-48000 are described on the following pages. A summary of the S-100 Bus signals is included in Appendix B.

Address Bus

The address bus consists of 24 lines used to select a memory location or an input/output device during a bus cycle. All 24 lines are active during a memory read, write or opcode fetch (M1) cycle unless the Memory Management Unit has been programmed for pass mode in which case the uppermost 8 bits (A16-A23) are forced to logic zero. The least significant byte of the address lines is active for input or output cycles. Address bus lines are enabled while ADSB* is inactive (no S-100 Bus DMA cycle in progress). The address bus lines are denoted as A0 through A23, with line A0 representing the least significant bit. Lines A0 through A7 compromise the least significant byte and lines A8 through A15 make up the "high" address byte with bits A16 through A23 constituting the extended address byte. Two octal-drivers and the Memory Management Unit are used to condition the lines in conformance with the characteristics required by the IEEE S-100 Bus standard.

Input Data Bus

There are eight input data lines which are enabled onto the CPU data bus when the enabling signal DIEN* is active. This signal is active under the following conditions:

1. AN EXTERNAL I/O CYCLE IS INITIATED.
2. AN EXTERNAL MEMORY CYCLE IS INITIATED.
3. AN EXTERNAL DEVICE INTERRUPTS THE CPU AND PLACES A VECTOR ON THE DATA BUS.

Output Data Bus

There are eight data output lines which are enabled by the signal DODSB*. A line driver conditions these lines to conform with the IEEE S-100 Bus standard.

Output Data Bus lines are designated DO0 through DO7, with line DO0 representing the least significant bit.

Status Bus

The status bus consists of eight output lines which define the current CPU bus cycle type. Seven of the eight lines defined in the S-100 Bus specification are utilized by the CPZ-48000. These lines are enabled while the enabling signal SDSB* is inactive. Status signals may be selected for full IEEE timing performance (latched mode) or for Z80 timing (transparent). This selection is made through jumper option JI. An octal latch/line driver is used to condition all lines of the Status Bus in conformance with the IEEE S-100 Bus standard. The seven lines of the Status Bus are:

Status	Function
sMEMR	Memory Read
sM1	Opcode Fetch
sINP	Input
sOUT	Output
sWO*	Write cycle
sINTA	Interrupt acknowledge
sHLTA	Halt acknowledge

The status signal SXTRQ* (16-bit data transfer request) is not used in the CPZ-48000 and is left open. The remaining Status Bus lines are described in the following paragraphs.

sMEMR (Memory Read)

sMEMR is a status signal indicating that a memory read cycle is in progress. This signal is valid during a normal memory read cycle (memory read or opcode fetch cycle).

sM1 (Opcode Fetch)

sM1 is a status signal indicating that a memory read/opcode fetch cycle is in progress.

sINP (Input)

sINP is a status signal indicating that a peripheral device read cycle is in progress.

sOUT (Output)

sOUT is a status signal indicating that a peripheral device write cycle is in progress.

sWO* (Write Cycle)

sWO* is a status signal indicating that a write cycle is in progress, wherein data is transferred from an S-100 Bus master to a slave.

sINTA (Interrupt Acknowledge)

sINTA is a status signal indicating that an interrupt acknowledge cycle is in progress.

sHLTA (Halt Acknowledge)

sHLTA is a status signal indicating that the CPU is in a halt state.

Control Input Bus

The Control Input Bus consists of six signals, five of which are used in the CPZ-48000. These lines allow S-100 Bus slaves to synchronize the CPZ-48000 with conditions internal to the bus slave, to request the relinquishment of the S-100 Bus (DMA request) and to disable the CPU from the S-100 Bus. The signals are conditioned by pull-up resistors and Schmitt-trigger input receivers.

The five lines of the Control Input Bus are:

Line	Function
RDY	Slave ready
XRDY	Special ready
INT*	Maskable interrupt request
NMI*	Non-maskable interrupt request
HOLD*	DMA request

These lines are described in the following paragraphs.

RDY (Slave Ready)

This control line is used by S-100 Bus slaves to suspend bus cycles by inserting wait states in a CPU cycle. Slaves may connect to this line by using an open-collector driver.

XRDY (Special Ready)

This control line is used as a special ready line to accommodate devices such as front panels. Only one slave device should connect into the XRDY line. This line also suspends bus cycles by introducing wait states to the CPU.

INT* (Maskable Int. Req.)

This control line is used to request service from the CPU on an interrupt basis. The INT* line is enabled (unmasked) or disabled (masked) under software control. When the INT* line is activated, the CPU responds with an acknowledge signal and subsequently gates the

opcode or vector information asserted on the bus by the bus slave initiating the interrupt. Interrupt may be asserted on the INT* line by the SIO, PIO or the 9519A interrupt controller. Logic is provided to sense these conditions and to respond appropriately. INT* should be asserted as a continuous level and held active until a response is received.

NMI* (Non-maskable Int. Req.)

This control line is used to request service from the CPU on an interrupt basis. The NMI* is non-maskable, meaning it is always enabled. When an interrupt occurs on NMI*, a CPU acknowledge cycle is not generated.

Normally, only critical signals are connected to the NMI* line. The CPZ-48000 provides the option to connect the S-100 Bus signal PWRFAIL* to the NMI* line via a jumper option. NMI* is sensed on a signal edge transition.

HOLD* (DMA Request)

This control line is used by S-100 temporary bus masters to request control of the S-100 Bus from the CPZ-48000. This line may be disabled under software control through the 9517A controller. When enabled, a DMA cycle may be initiated by asserting this line. The 9517A DMA controller will respond with the signal pHLDA when the cycle is initiated, and will relinquish control to the temporary bus master.

Control Output Bus

The control output bus consists of six lines, one of which is optional. These lines are enabled when the enabling signal CDSB* is inactive. A line driver is used to condition these lines to conform with the characteristics required by the IEEE S-100 Bus standard.

The six lines of the Control Output Bus are:

Line	Function
pSYNC	Cycle start
pSTVAL*	Status valid
pDBIN	Read strobe
pWR*	Write strobe
pHLDA	Hold acknowledge
pWAIT	Wait (Optional)

These lines are described in the following paragraphs.

pSYNC (Cycle Start)

pSYNC is a control signal which indicates the start of a new bus cycle. The signal becomes active when an I/O cycle, memory cycle, DMA read or DMA write cycle occurs. The signal remains active for approximately one bus clock in accordance with the IEEE S-100 Bus standard. pSYNC does not become active during a refresh cycle.

pSTVAL* (Status Valid)

pSTVAL* is a control signal which indicates that address, Data and Status signals have stabilized on the bus during the current bus cycle. It becomes active on the first CPU clock cycle after pSYNC becomes active, and goes inactive on the first CPU clock cycle after the bus cycle is complete. By using this signal as the latching signal, the address, data, and status signal timing will conform to the timing specified in the IEEE standard.

pDBIN (Read Strobe)

pDBIN is a control signal which gates data arriving on the CPU data bus from an external source. Header jumper option JC is provided to specify the pulse width and timing for this signal. Two options are available:

a. FULL IEEE TIMING CONFORMANCE: In this option, pDBIN goes active at a specified time after pSTVAL* goes active. This presents the smallest read access time window available. A single clock cycle duration is typical.

b. Z80 TIMING: In this option, pDBIN goes active when the Z80 read signal goes active, thereby giving the user a maximum read access time window. This is typically one and one-half clock cycles in duration.

pWR* (Write Strobe)

pWR* is a control signal which performs the function of a write strobe to write data from the CPU data bus to an addressed peripheral or memory device. pWR* goes active at the specified time after pSTVAL goes active for I/O write cycles, DMA memory write cycles and CPU memory write cycles.

pHLDA (Hold Acknowledge)

pHLDA is a control signal which is active when the CPZ-48000 relinquishes the address, data, control and status buses in response to a temporary master DMA request. This signal is generated by the 9517A DMA controller, channel 0 DMA acknowledge output.

pWAIT (Wait [optional])

pWAIT is a control signal which is active when any wait condition is active within the CPZ-48000. Thus, pWAIT goes active when either of the two S-100 Bus wait lines (RDY or XRDY) go active, the FDC programmed I/O wait state generator goes active or when the 9519A interrupt controller "pause" signal goes active (indicating that an interrupt cycle is in progress and the daisy chain priority is being resolved). pWAIT is optional and may be connected or disconnected via a jumper option. pWAIT is not a signal required by the IEEE S-100 Bus standard.

DMA Control Bus

The DMA Control Bus consists of eight input lines. Four of these are activated as required for the permanent bus master. The remaining four lines are utilized to isolate the CPU from the S-100 when the permanent bus master relinquishes control to the temporary bus master. The disable lines are connected to schmitt-trigger input receivers to provide noise immunity. The conditioned signals then disable the respective output line drivers. The DMA arbitration lines

are used by the temporary masters to determine which temporary master has the use of the bus during a DMA cycle. The permanent bus master need not arbitrate. The eight DMA Control Bus lines are:

Line	Function
DMA0*	DMA arbitration line
DMA1*	DMA arbitration line
DMA2*	DMA arbitration line
DMA3*	DMA arbitration line
ADSB*	Address disable
DODSB*	Data out disable
SDSB*	Status disable
CDSB*	Control output disable

Vector Interrupt Bus

The Vectored Interrupt Bus consists of eight lines, designated VIO* through V17*. VIO* is treated as the highest priority interrupt line. These lines should be asserted as levels, and should remain asserted until a response is received.

The Vectored Interrupt Bus lines are connected to interrupt option jumpers to connect the appropriate lines to the 9519A interrupt controller. This device then masks or unmasks the interrupts, prioritizes the requests, and asserts the INT* signal to the CPU.

Utility Bus

The Utility Bus consists of eight lines. Output lines are conditioned by drivers to conform with characteristics required by the IEEE S-100 Bus standard. The eight Utility Bus lines are:

Line	Function
ϕ (clock)	System clock (output)
CLOCK	Clock (output)
MWRITE	Memory write strobe (output)
POC*	Power-on clear (output)
SLAVE CLR*	Slave clear (output)
RESET*	Reset (input/output)

Each of these Utility Bus signals are described in the following paragraphs.

ϕ (System Clock)

ϕ is the S-100 Bus system clock. ϕ has the same sense as the inverted CPU computer clock (BCLK).

CLOCK (Clock)

CLOCK is a 2 Megahertz Utility clock signal to be used by slave devices.

MWRITE (Memory write)

This line is optional on the CPZ-48000. It may be connected to the bus via jumper option JD, or this signal may be generated externally to the CPZ-48000, in which case the jumper would be omitted.

Logic is provided so that MWRITE is generated by either CPZ-48000 on-board signals (pWR* & sOUT) or by off-board signals if the status and control bus drivers are disabled. This signal is active during DMA and CPU memory write cycles.

*** N O T E ***

Care must be taken that the signal is generated at only one point in the system.

POC* (Power-on Clear)

The POC* line is active when initial power-up occurs on the S-100 Bus. When POC* is active, SLAVE CLR* and RESET* are asserted. POC* is guaranteed to stay active for at least 50 milliseconds.

SLAVE CLR* (Slave Clear)

SLAVE CLR* is the signal line which resets all slave devices on the S-100 bus. During power-on clear, this line is asserted by the CPZ-48000 power-on clear logic. External devices may assert RESET*

and, in doing so, assert SLAVE CLR* as well. RESET* is driven by an open-collector driver.

ERROR* (Error)

Error* is a signal generated by a slave device to indicate abnormal conditions such as parity error, CRC error, out of tape, etc. This line is connected to a jumper option where it may be selected as an interrupt source.

PWRFAIL* (Power Failure)

PWRFAIL* is a signal generated external to the CPZ-48000 to indicate that a power failure has occurred. This signal remains active until power is restored and POC* is active. The signal is available to the user via a jumper so that it may be connected to the NMI* line of the CPU.

System Power

The system power lines consist of all lines supplying unregulated power to the CPZ-48000 and other devices connected to the S-100 Bus. The nine System Power lines are:

Lines	Quantity
+8 VOLTS	2
+16 VOLTS	1
-16 VOLTS	1
GND	5

The +8 VOLT lines are connected to a +5 VDC regulator to supply +5 volt of regulated power to the CPZ-48000.

The +16 VOLT connects to a +12 VDC regulator and the two serial port connectors. The -16 VDC line connects to the two serial port connectors. The 16 volt lines are utilized on the serial ports for supplying power to RS-232C driver circuitry.

All ground lines are connected to the ground plane to provide a low impedance path from the S-100 Bus ground to the CPZ-48000 ground.

MANUFACTURER SPECIFIED LINES

The IEEE S-100 Bus standard reserves three of the 100 lines for special use by the manufacturer. The CPZ-48000 utilizes these lines. Two of these are required to implement the daisy chained priority interrupt expansion. The third supplies the Z80 refresh signal.

All lines may be connected through solder jumpers. See the section on Solder/Trace Cut Options.

The three Manufacturer specified lines are described in the following paragraphs.

IPROCESS* (Interrupt in Progress)

IPROCESS* is a bi-directional signal which indicates that an interrupt cycle is in process. This line is required to cascade external 9519A Universal Interrupt Controllers. IPROCESS* utilizes pin 65 of the S-100 Bus.

PCHAIN (Interrupt Priority)

PCHAIN is an output signal which indicates the priority level of the interrupt in progress. If it is high, the interrupt response action is passed to the next interrupt device in the serial interrupt structure. PCHAIN utilizes pin 21 of the S-100 Bus.

RFSH* (Refresh)

RFSH* is the Z80 refresh signal buffered for use by external dynamic RAM memory devices connected to the S-100 Bus.

Reserved Lines

Five of the S-100 Bus lines are reserved for future use by the IEEE specification. The CPZ-48000 makes no connection to these lines.

**** OPERATING INSTRUCTIONS ****

Instructions are given herein to configure the CPZ-48000 from both the hardware and software standpoint. The user will be pleased to find that minimal setup procedures are required.

HARDWARE SETUP INSTRUCTIONS

The hardware is configured via jumper options and solder/trace cut areas. The solder/trace cut areas are referred to as PJX, where X is the area designator. These jumpers are by nature rarely reconfigured. PJX options are located on the "solder" side of the board. The jumper options referred to as JX, where X is the jumper designator, gives the user flexibility in setting up the CPZ-48000 for a multitude of applications. Jumper options are located on the "component" side of the board. Instructions are also included on connecting the personality boards to the CPZ-48000.

JUMPER OPTIONS

Refer to figure 1 to locate the JX header positions. The JX jumper blocks are listed as follows:

JA - FLOPPY DISK CONTROLLER CLOCK SELECT
JB - EPROM SELECT
JC - INTERRUPT SIGNAL SOURCE SELECT
JD - CONNECT "MWRITE" TO S-100 BUS
JE - IEEE/Z80 TIMING SELECT
JF - S-100 BUS STATUS (IEEE or TRANSPARENT SELECT)

JA

The FDC requires a 2Mhz clock when operating with 8-inch drives and a 1Mhz clock when operating with 5-1/4-inch drives. To select the 2Mhz clock, set the jumper provided to position 2-1. To select the 1Mhz clock, set the jumper provided to position 3-2.

```
   [ JA ] block
    +---+
1   | O | 2 MHz
2   | O |
3   | O | 1 MHz
    +---+
```

JB

Either a 2716 or 2732 EPROM may be used with the CPZ-48000. To configure the board for a 2732 EPROM, set the jumper provided to position 2-1. This connects address line A11 as an input to the 2732. To configure the board for a 2716 EPROM, set the jumper provided to position 3-2. This connects +5VDC to the 2716 input.

```
     [ JB ] block
     +---+
1    | O |  A11
2    | O |
3    | O |  +5 Vdc
     +---+
```

JC

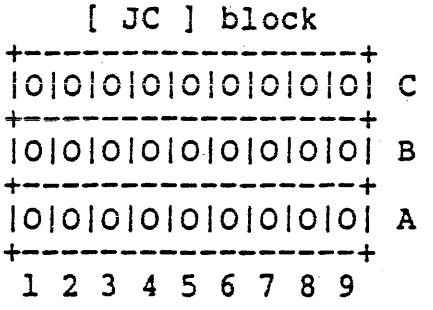
JC may be configured to select various signals as inputs to the interrupt controller. Jumpers are provided to select one of two signals available for each of 9 inputs. Wire-wrap or other means of interconnection may be used to select a signal in a different order from that assigned to the jumper block. This is clarified below:

Connection Table

Pin	A	B	C
1	V0*	IREQ0*	RTCLK
2	V1*	IREQ1*	FINT
3	V2*	IREQ2*	EDMA1*
4	V3*	IREQ3*	EDMA2*
5	V4*	IREQ4*	EDMA3*
6	V5*	IREQ5*	PINT*
7	V6*	IREQ6*	SERR*
8	V7*	IREQ7*	(SPARE)
9	PWRFAIL*	INMI*	NMI*

```
                  ^          ^          ^
                  |          |          |
Source Signal ----+          |          |
Input to interrupt Controller -+         |
Source Signal ---------------------------+
```

** N O T E ** (B-9 is input to NMI* of CPU)



EXAMPLES:

1) To connect S-100 Bus Vector line V5* to the interrupt controller, install a jumper from position A6 to B6.

2) To connect Floppy interrupt signal FINT* to the interrupt controller, install a jumper from C2 to B2.

3) To connect the parallel port interrupt line to the highest priority interrupt input (IREQ0), install wire-wrap or any other adequate interconnection means from C6 to B1.

**** N O T E ****

a.) Highest priority input is IREQ 0 and the lowest is IREQ 7.
b.) NMI and PWRFAIL are sources to the CPU non-maskable interrupt input.
c.) Signal source definition are as follows:

Vx = S-100 Bus vectored interrupt (X = 0 --> 7)
PWRFAIL = S-100 Bus power fail
RTCLK = Real Time Clock
FINT = Floppy interrupt
EDMAX = Channel X end of DMA process (X = 1 --> 3)
PINT = Parallel port interrupt
SERR = S-100 Bus error
NMI = S-100 Bus non-maskable interrupt

JD

The CPZ-48000 may be configured to output S-100 Bus signals in compliance with the IEEE specifications for the S-100 Bus timing, or it may be configured to output the bus signals in Z80 mode. The selection is made via jumpers JD and JF. To select IEEE timing, jumper position 2-3 of JD. To select Z80A timing, jumper position 1-2 of JD.

```
  [ JD ] block
   +---+
3  | O | IEEE
2  | O |
1  | O | Z80
   +---+
```

JE

The signal "MWRITE" may be generated on the CPZ-48000 or it may be generated from signals external to the CPZ-48000 like a front panel. In any case, the signal should be sourced by one device only. If the CPZ-48000 is to be the source of the signal, install the jumper provided on jumper block JE, otherwise, leave the jumper off.

```
[ JE ] block
 +-+
 | |
 |O|
 | |
 |O|
 | |
 +-+
```

JF

The S-100 Bus status signals may be output from the CPZ-48000 in latched mode which makes timing conform to the IEEE specification or may be output in transparent mode which makes the timing correspond to that of the Z80. To select Z80 timing, jumper position 2-3 of JF. To select IEEE timing, jumper position 1-2 of JF.

```
  [ JF ] block
   +---+
3  | O | Transparent
2  | O |
1  | O | Latched
   +---+
```

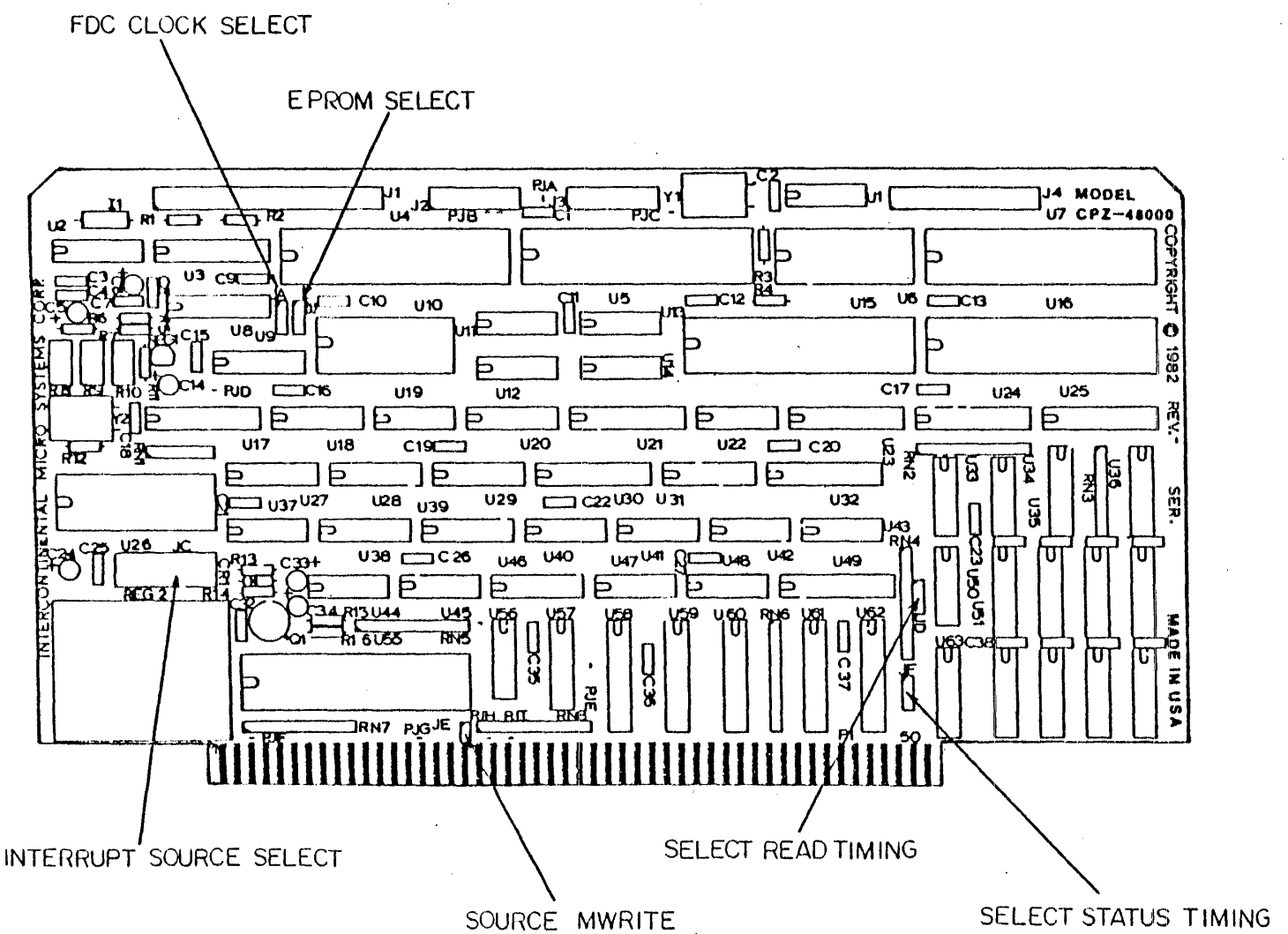


FIGURE 1

JUMPER OPTIONS

SOLDER/TRACE CUT OPTIONS

Refer to figure 2 to locate the PJX solder/trace options. The PJX options are listed as follows:

PJA - SIO PORT A clock source select
PJB - SIO PORT B clock source select
PJC - CONNECT INTERRUPT IN PROCESS to S-100 Bus
PJD - CONNECT INTERRUPT PRIORITY CHAIN to S-100 Bus
PJE - CONNECT Z80 REFRESH to S-100 Bus
PJF - CONNECT S-100 Bus GROUND to PCB ground plane

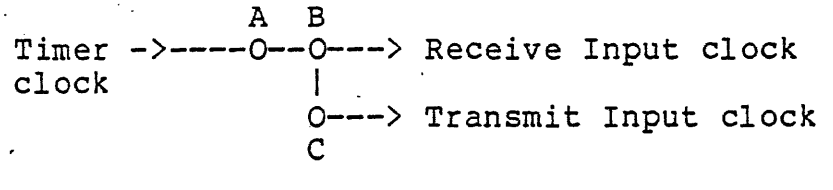
PJA

The CPZ-48000 comes configured so that the SIO ports receive their baud rate clocks from an on-board programmable timer. The board could be reconfigured to source the clocks from the SIO serial port connectors. Such is the case when synchronous modems connect to the serial ports. The modem provides a clock to the SIO. Furthermore, the modem may receive the clock from the on-board timer, condition the clock and return it to the input of the SIO. The transmit and receive clocks may be sourced separately on Port A. All combinations are possible through this jumper.

To source SIO PORT A inputs from the SIO connector only, cut the trace from PJA 'a' to PJA 'b'. The source can now be connected through the personality board on either PIN P2-2 or P2-3.

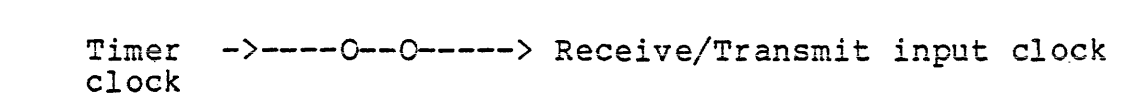
If the SIO PORT A inputs are to be sourced separately from the SIO connector, cut the trace from PJA b to PJA c. The receive clock is now input on P2-3 and the transmit clock is input on P2-2.

[PJA] area



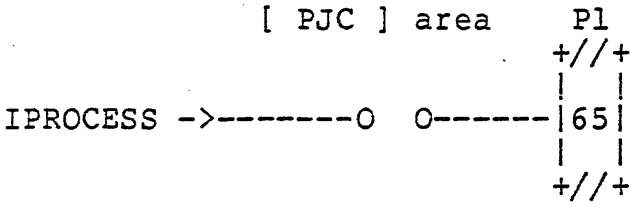
PJB

To source SIO Port B input from the SIO connector only, cut the trace at PJB. The source can now be connected through the personality board on pin P3-3.



PJC

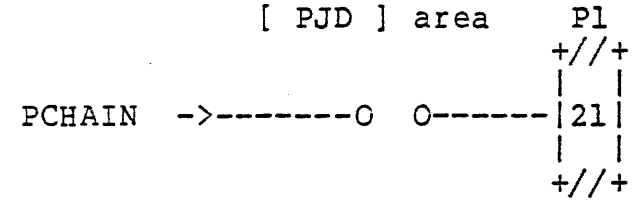
The CPZ-48000 may connect to off-board devices with priority interrupt structures which comply with the Advanced Micro Digital Universal Interrupt Controller AM9519A method of resolving interrupt priority level. The method consists of serially chaining interrupt devices via a signal referred to as "PCHAIN" and connecting in parallel the signal "IPROCESS". The CPZ-48000 is factory configured so that both these signals are NOT connected to the S-100 Bus. Solder a jumper in PJC if the interrupt structure is to be extended to other boards outside of the CPZ-48000.



PJD

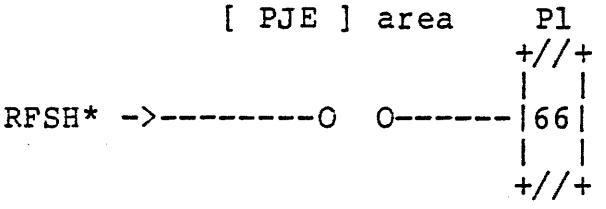
See PJC.

Solder a jumper in PJD if the interrupt structure is to be extended to other boards outside of the CPZ-48000.



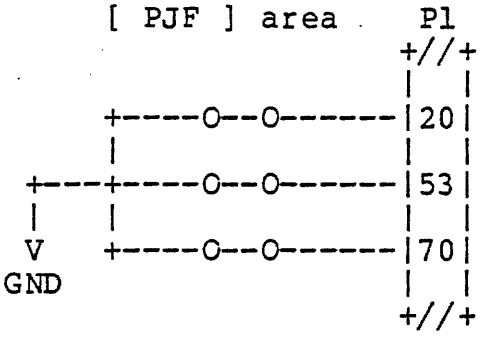
PJE

If the S-100 Bus dynamic RAM memory boards require the Z80 refresh signal for proper operation, PJE may be connected to provide that signal.



PJF

Some S-100 Bus boards utilize pin 20, 53, and 70 for signals other than ground. The IEEE specification requires that these be connected to ground. If a board is installed in the bus and any of these pins are used for other than ground, the corresponding traces at PJF must be cut.



Qume Datatrack 8 jumper options

Drive Desiginator	Drive Option	
C	closed	
D	open	
DC	open	
2S	open	
DS1	drive select for A --	
DS2	drive select for B	} we treat the drive as
DS3	drive select for C	} one big drive for double
DS4	drive select for D --	sided operation.
T40	open	
HA	open	
Y	closed	
DL	open	
DS	closed	

SHUNT	
A	closed
B	closed
X	open
R	closed
I	closed
Z	open
HL	open

All other drive jumpers are left as is from the factory.

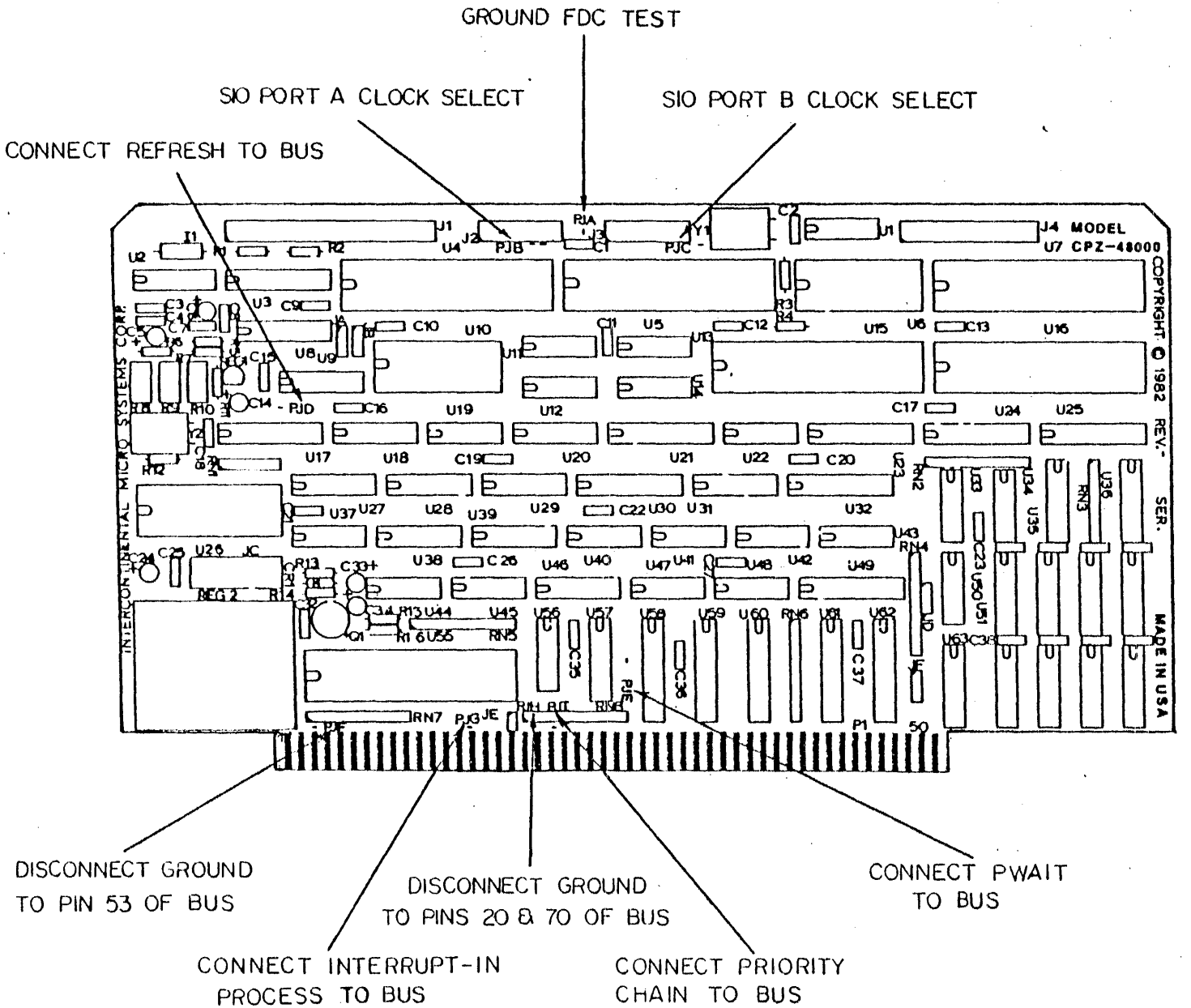


FIGURE 2
SOLDER/TRACE CUT OPTIONS

PERSONALITY BOARD INTERCONNECTION INSTRUCTIONS

The CPZ-48000 has four connectors at the top of the board numbered J1 through J4. These are listed below:

J1 - FDC Connector
J2 - SIO Port A Connector
J3 - SIO Port B Connector
J4 - PIO Connector

These are typically connected to peripheral devices through personality boards which are small printed circuit boards customizing the above listed devices to a variety of peripherals.

Most S-100 Bus chassis provide a jumper plate at the rear of the chassis to which peripheral connectors are installed. Typically, the connectors are of the ITT CANNON DB25 type. The personality boards provided by ICM are boards with DB25 connectors at one end and header plug connectors at the other. The DB25 connector end is to be installed in the cutouts provided on the connector plate. Flat ribbon cable then connects the CPZ-48000 connector to the personality board. See figure 3 showing a personality board installation.

The FDC personality boards are provided with connector adapters. These adapters reconfigure the connection from DB25 type connectors to header plug or edge card type connectors to provide a means for the user to utilize standard controller to drive cables. See figure 4 showing the addition of a connector adapter.

At a minimum, the FDC and SIO Port B personality boards must be installed. The instructions follow:

1.- Select a DB25 connector cutout at the rear of the chassis for the FDC personality board.
2.- Insert and hold the FDC personality board in the cutout. External to the chassis, plug in the desired connector adaptor and hold in place.
3.- Install #6 nuts, washers and bolts passing the bolts through the connector adapter and through the personality board's DB25 connector.
4.- Install the flat ribbon cable provided at the personality board and at the CPZ-48000, connector J1.
5.- Follow the above procedure, except that an adapter is not used, for the SIO Port B personality board.
6.- Install cables from the chassis connectors to the respective peripherals.

**** SOFTWARE SECTION ***

This section of the manual describes the Software Interface for the CPZ-48000.

PROM Monitor

The CPZ-48000 is shipped with a 2 Kbyte PROM Monitor with basic memory alter functions, I/O examine functions, Breakpoint facilities, and Disk drive boot function. The terminal baud rate is sensed automatically by pushing carriage returns until the PROM monitor signs on. Channel B is the main console port, while channel A is the printer port. Channel A defaults to 9600 baud for the printer. User programs may be written to change the baud rate on the fly if needed. Baud rates supplied for the terminal are as follows:

76800,38400,19200,9600,4800,2400,1200,600,300 baud.

Below is a description of the built-in Monitor commands and their functions. Commands may be either a single letter, single letter followed by 1, 2 or 3 parameters, or double letter commands followed by 1, 2 or 3 parameters and depends upon the function desired.

Basic PROM Commands

*** Note: *** <cr> = carriage return
all entries are in hex.

---- Register definitions ----
A=accumulator, F=flags, B=register B, C=register C
D=register D, E=register E, H=register HL
X=register IX, Y=register IY, P=program counter
I=interrupt register, N=interrupt flip-flop

Letter	Function	Description
A	not used	
B<cr>	Boot disk drive A:	Load operating system on drive A: (CP/M disk)
Cxxxx,yyyy,zzzz<cr>	Compare memory	Will compare the block of memory starting with xxxx to yyyy with zzzz.

DMxxxx,yyyy>cr>	Dump Memory	Will display memory from xxxx to yyyy hex.
DMxxxx,S100<cr>		Will dump memory starting at xxxx with a swath of 100.
DR<cr>	Display Registers	Will display all Z-80 CPU registers.
E	not used	
Fxxxx,yyyy,zz<cr>	Fill memory	Will fill memory starting at xxxx to yyyy with the hex byte zz.
G<cr>	Go command	Will execute the program pointed to by the break-point PC value without trace or breakpoint active.
Gxxxx<cr>	Go at address	Will set the Program counter to address xxxx and begin execution there.
Gxxxx/yyyy<cr>	Go with Breakpoint	Begin execution at address xxxx with a breakpoint at address yyyy.
G/yyyy<cr>	Go with Breakpoint	Use present Program counter value to execute until address yyyy is reached.
Hxxxx,yyyy<cr>	Hex Math	Display the hex SUM and Difference of xxxx and yyyy
I	not used	
J	not used	
K	not used	
L	not used	
Mxxxx,yyyy,zzzz<cr>	Move memory	Will move the memory contents xxxx to yyyy stating at zzzz.
N	not used	
Oyy,xx<cr>	Output to port	Will output the byte xx to port yy hex.
P	not used	
Qxx<cr>	Query input port	Will display the hex and binary contents of port xx hex.

R<cr>	Read disk	Will read the diskette in drive A:, track 0 sector 1 starting location 0000 hex of memory.
SMxxxx<cr>	Substitute Memory	Allows the substitution of memory contents starting at xxxx. Carriage return will abort, space bar advances to next location.
SRx<cr>	Substitute Register	Allows the substitution of all break point register values and flags as shown in notes.
T	not used	
U	not used	
Vxxxx,yyyy,zzzz<cr>	Verify memory	Allows the verifying of memory block xxxx to yyyy with the contents of memory at zzzz. will display the differences.
W<cr>	Write disk	Will write memory contents at location 0000 hex of memory onto the diskette in drive A:
X	not used	
Y<cr>	Display Help Menu	Will display an abbreviated HELP menu on terminal.
Zxxxx,yyyy	Zero memory	Will zero memory between xxxx and yyyy.

PROM Monitor Display Options

The monitor has several display options which allow the control of screen dumps and control of listings using a printer. These options are listed below.

Function	Option	Description
Memory Dumps -	Control-S	Stops Display scroll.
-	Control-Q	Starts Display scroll.
-	Esc key	Aborts dump and returns to command level.
Printer listing -	Control-P	Enables console dumps to printer. This is a toggle function, where a second control-P will stop printer listing.

(NOTE) Control P option valid only while in the monitor command mode.

I/O Port Address Assignments

The CPZ-48000 uses the last 128 I/O ports assignment of it's 256 I/O port address space for use with it's on-board peripheral chips. Below is a breakdown of these i/o ports by port function and it's corresponding address in hex.

[Serial Port A and B Assignments]

SIO Port A Data Reg.	80 Hex
SIO Port A Control Reg.	81 Hex
SIO Port B Data Reg.	82 Hex
SIO Port B Control Reg.	83 Hex

[Floppy Disk Controller Assignment]

FDC Command/Status Reg.	90 Hex
FDC Track Reg.	91 Hex
FDC Sector Reg.	92 Hex
FDC Data Reg.	93 Hex

[Parallel Port A and B Assignment]

PIO Port A Data Reg.	A0 Hex
PIO Port A Control Reg.	A1 Hex
PIO Port B Data Reg.	A2 Hex
PIO Port B Control Reg.	A3 Hex

[Timer Port Assignments]

Timer Channel 0	B0 Hex
Timer Channel 1	B1 Hex
Timer Channel 2	B2 Hex
Timer Control Reg.	B3 Hex

[Interrupt Controller Assignments]

Interrupt Select Reg.	C0 Hex
Interrupt Command Reg.	C1 Hex

[Control Registers]

Prom/Boot Reg.	D0 Hex
Deselect Window Reg.	D1 Hex
FDC Drive Select Reg.	D2 Hex
FDC Wait Reg. (program data xfer use)	D3 Hex

[Memory Management Registers]

MMU Address Reg 1	E0 Hex
MMU Address Reg 2	E1 Hex
MMU Address Reg 3	E2 Hex
MMU Address Reg 4	E3 Hex
MMU Address Reg 5	E4 Hex
MMU Address Reg 6	E5 Hex
MMU Address Reg 7	E6 Hex
MMU Address Reg 8	E7 Hex
MMU Address Reg 9	E8 Hex
MMU Address Reg 10	E9 Hex
MMU Address Reg 11	EA Hex
MMU Address Reg 12	EB Hex
MMU Address Reg 13	EC Hex
MMU Address Reg 14	ED Hex
MMU Address Reg 15	EE Hex
MMU Address Reg 16	EF Hex

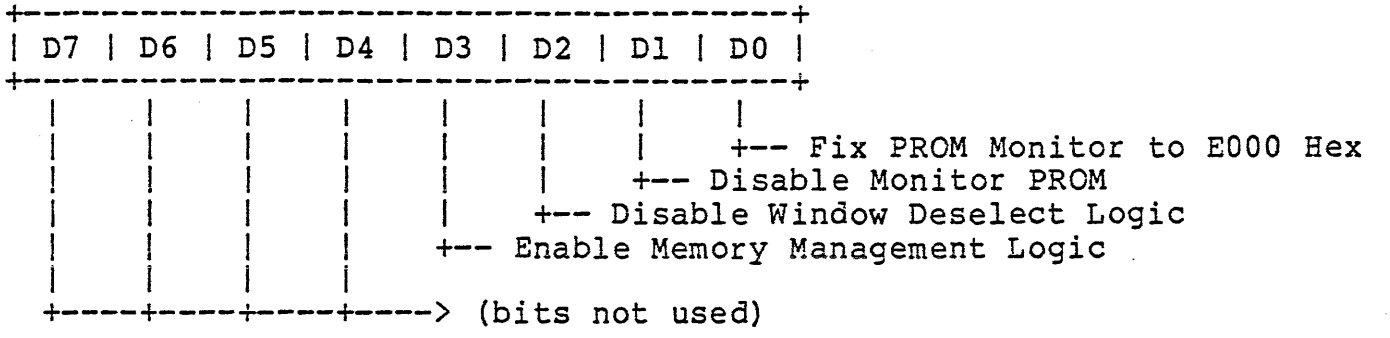
[Direct Memory Access Registers]

DMA Base/Current Address Reg. 0	F0 Hex
DMA Base/Current Word Count Reg. 0	F1 Hex
DMA Base/Current Address Reg. 1	F2 Hex
DMA Base/Current Word Count Reg. 1	F3 Hex
DMA Base/Current Address Reg. 2	F4 Hex
DMA Base/Current Word Count Reg. 2	F5 Hex
DMA Base/Current Address Reg. 3	F6 Hex
DMA Base/Current Word Count Reg. 3	F7 Hex
DMA Status/Command Register	F8 Hex
DMA Write Request Register (software)	F9 Hex
DMA Write Single Mask Reg.	FA Hex
DMA Write Mode Reg.	FB Hex
DMA Clear Byte Pointer Flip-Flop	FC Hex
DMA Master Clear/Read Temp. Reg.	FD Hex
DMA (not used)	FE Hex
DMA Write All Mask Reg.	FF Hex

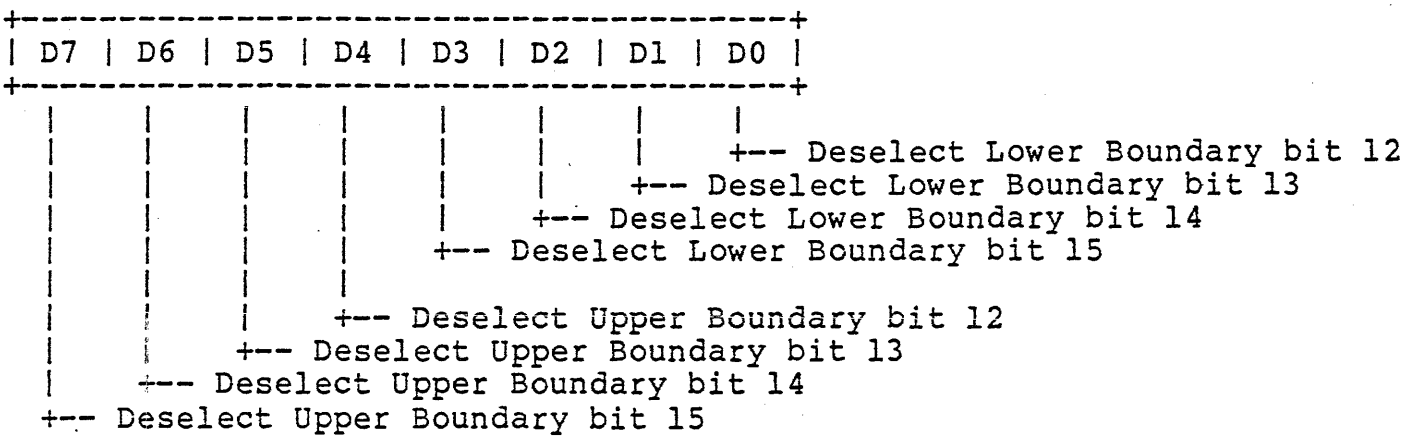
Control Register Bit Assignments

This is a description of the Control Register Bits used on the CPZ-48000 board.

[PROM / Boot Register (Port D0 Hex)]



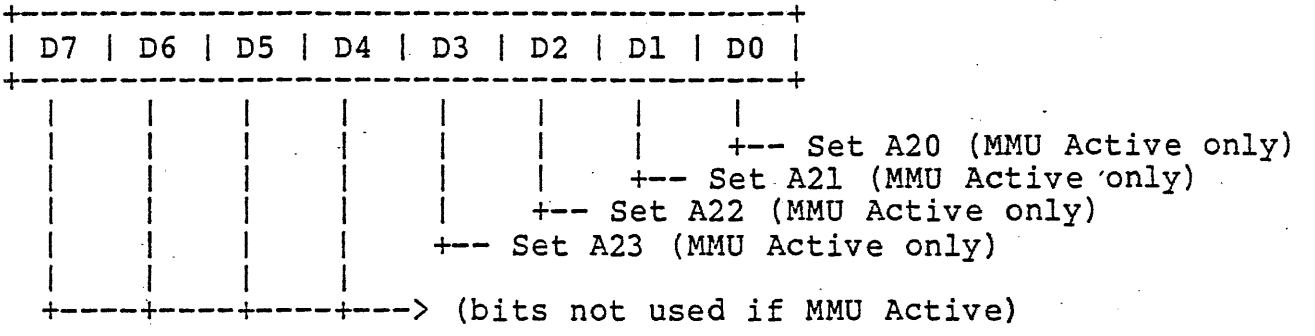
[Deselect Memory Window (Port D1 Hex)]



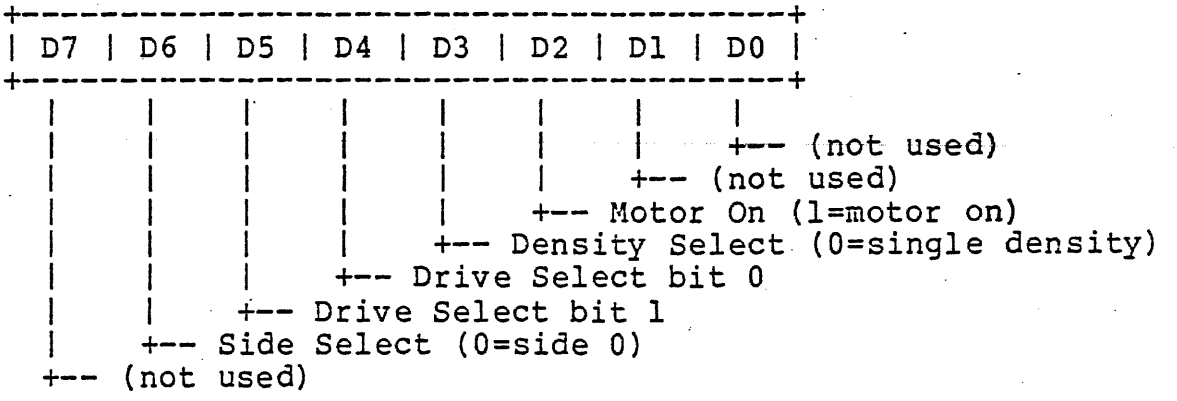
**** N O T E ****

The Deselect Window logic has a secondary function which is only active if the PROM Monitor is not active. The lower 4 bits of this control register sets the range for the extended groups of each 1 megabyte of extended address lines A20 to A23. Below is a table showing the bit assignments for this function.

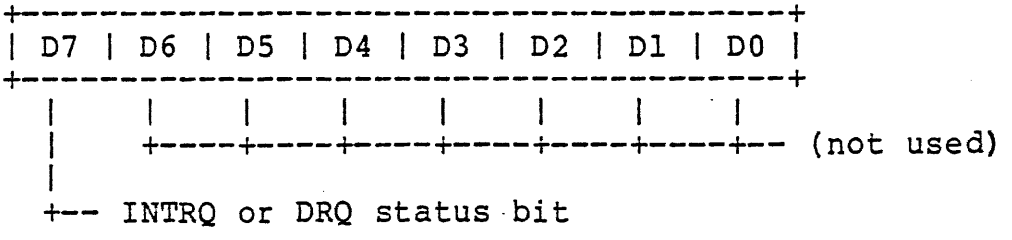
[Extended Megabyte Set Register (Port D1 Hex)]



[FDC Drive Select Register (Port D2 Hex)]

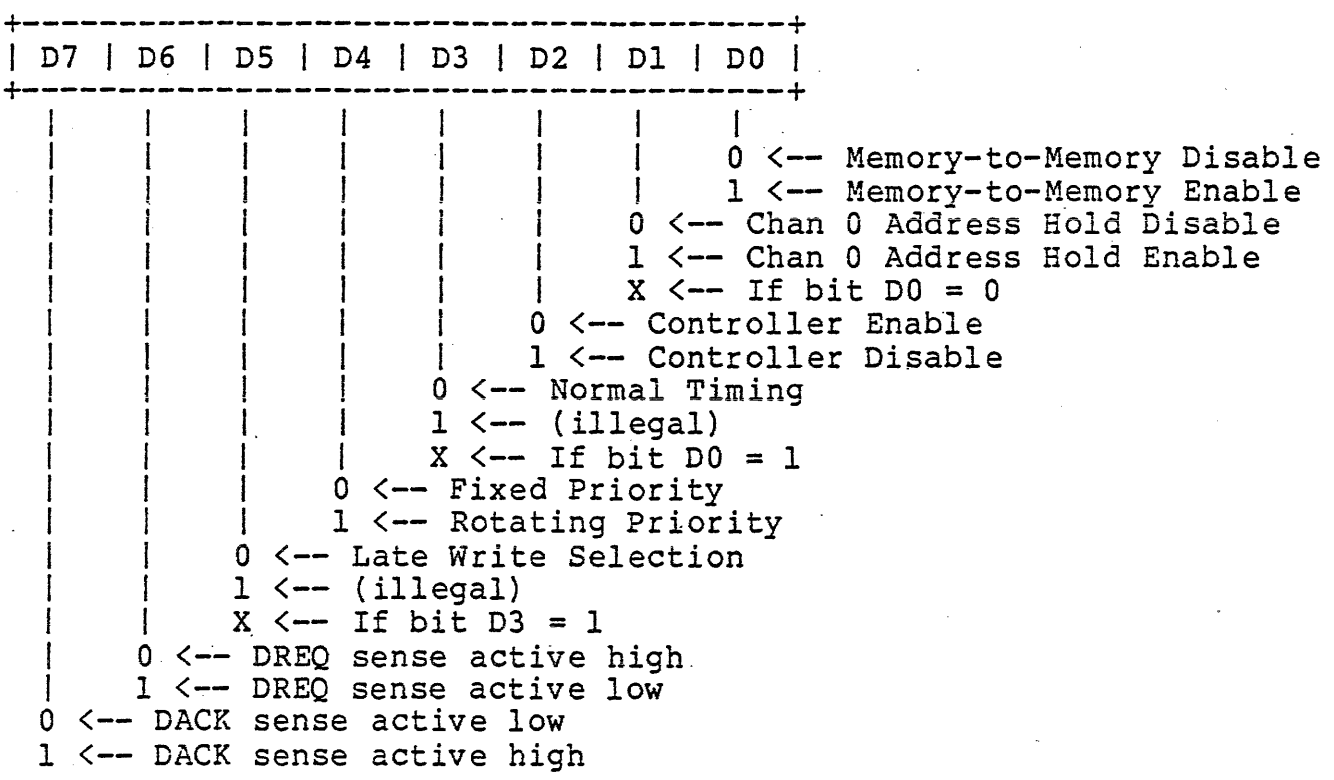


[FDC Wait Register (Port D3 Hex)]

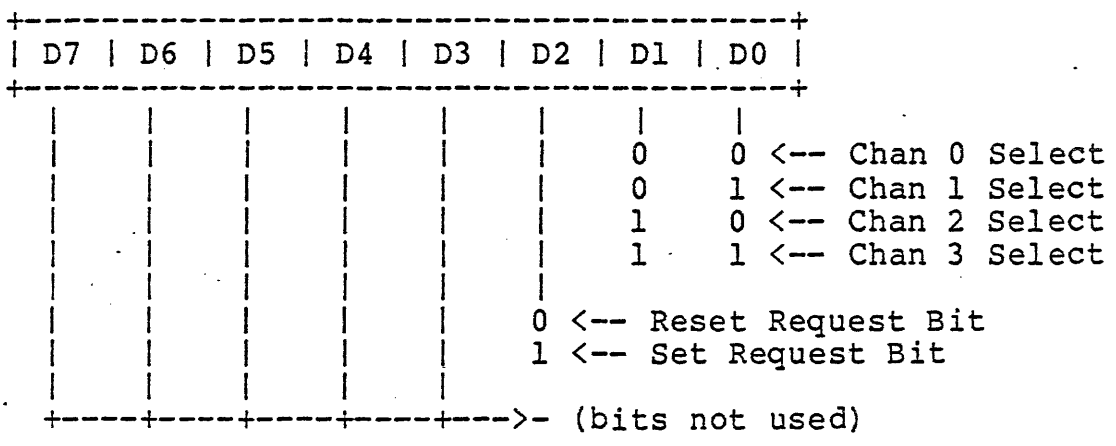


DMA Register Bit Assignments

[Command Register]



[Request Register bits]



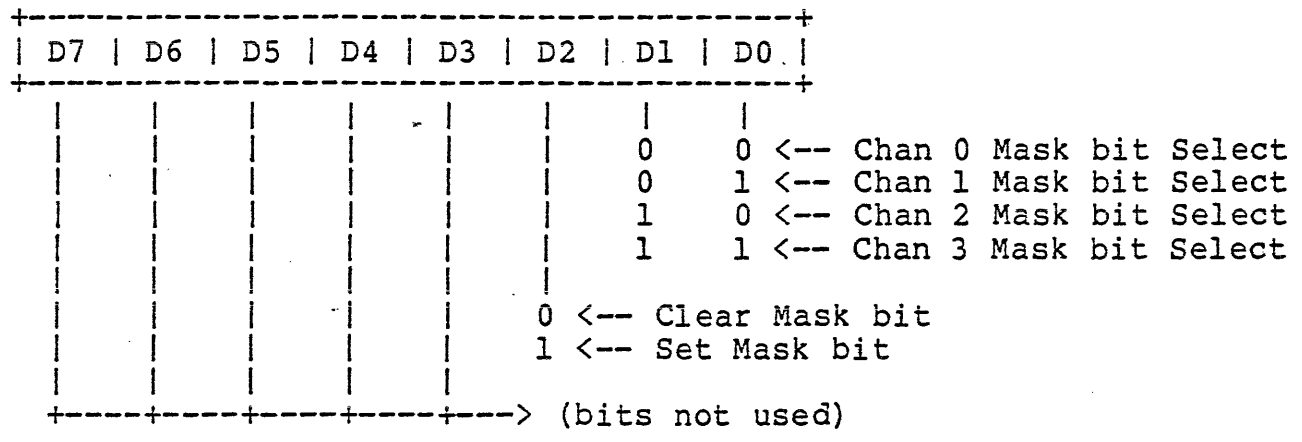
[Mode Register Bit Assignments]

```
+-----------------------------------------+
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
+-----------------------------------------+
  |    |    |    |    |    |    |    |
  |    |    |    |    |    |    0    0 <-- Chan 0 Select
  |    |    |    |    |    |    0    1 <-- Chan 1 Select
  |    |    |    |    |    |    1    0 <-- Chan 2 Select
  |    |    |    |    |    |    1    1 <-- Chan 3 Select
  |    |    |    |    |    0    0 <-- Verify Transfer (not used)
  |    |    |    |    |    0    1 <-- Write Transfer
  |    |    |    |    |    1    0 <-- Read Transfer
  |    |    |    |    |    1    1 <-- (illegal)
  |    |    |    |    |    X    X <-- If bits D6 & D7 = 11
  |    |    |    |    0 <-- Disable Autoinitialize
  |    |    |    |    1 <-- Enable Autoinitialize
  |    |    |    0 <-- Select Address Increment
  |    |    |    1 <-- Select Address Decrement
  0    0 <-- Demand Mode Select
  0    1 <-- Single Mode Select
  1    0 <-- Block Mode Select
  1    1 <-- Cascade Mode Select
```

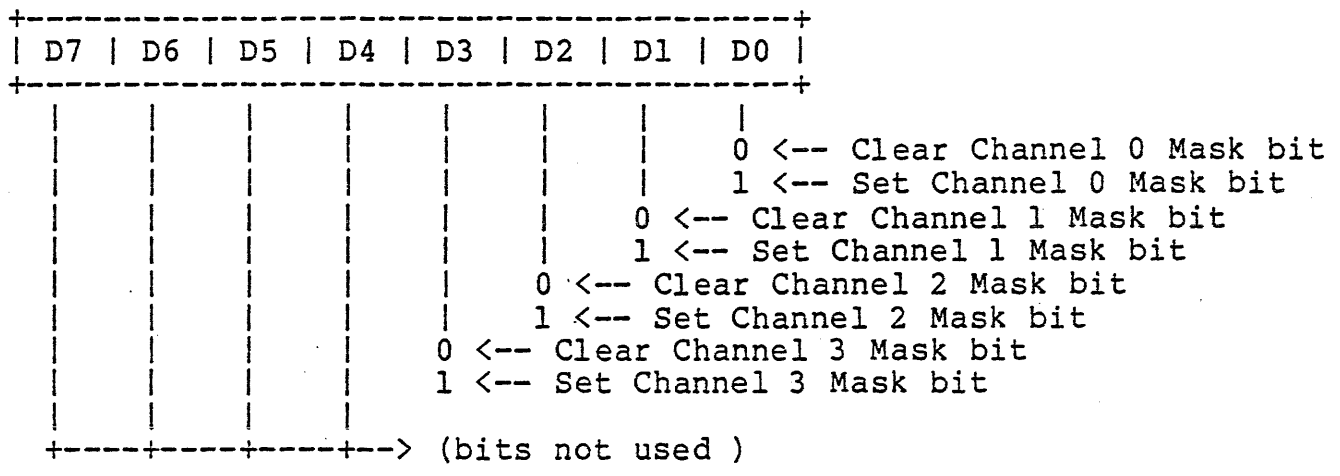
[Status Register Bit Assignments]

```
+-----------------------------------------+
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
+-----------------------------------------+
  |    |    |    |    |    |    |    |
  |    |    |    |    |    |    |    1 = Chan 0 has reached T.C.
  |    |    |    |    |    |    1 = Chan 1 has reached T.C.
  |    |    |    |    |    1 = Chan 2 has reached T.C.
  |    |    |    |    1 = Chan 3 has reached T.C.
  |    |    |    |
  |    |    |    |
  |    |    |    1 = Chan 0 is Requesting
  |    |    1 = Chan 1 is Requesting
  |    1 = Chan 2 is Requesting
  1 = Chan 3 is Requesting
```

[Mask Register (single mask bit) Assignments]



[Mask Register (all mask bits) Assignment]



Serial Port A and B Software Description

Both serial ports A and B must be initialized after a system reset is performed before they will communicate with any terminals or the like. Each channel has a set of registers which program the device for a certain function. As we are only concerned with programming each channel for standard RS-232C interfacing, we will not describe the other functions that each channel contains here. For further information about the SDLC/HDLC functions, refer to the ZILOG support chip manuals.

Below is a software example for initializing the SIO ports A and B for standard RS-232C interfacing.

```
CMNDA   EQU     81H             ;command port chan A
CMNDB   EQU     83H             ;command port chan B
;
;init channel A:
;get length of init table in reg b
;get command port into reg c.
;
INITA:  LXI     B,(CHANAE-CHANA) SHL 8 OR CMNDA
        LXI     H,CHANA         ;point to chan A init table
        OTIR                    ;block i/o send it
;
;init channel B:
;get length of init table in reg b,
;get command port into reg c.
;
INITB:  LXI     B,(CHANBE-CHANB) SHL 8 OR CMNDB
        LXI     H,CHANB         ;point to chan B init table
        OTIR                    ;block i/o send it
        RET
;
;init tables for channel A and B
;
CHANA:  DB      18H,04H         ;reset A, write reg 4
        DB      4CH,01H         ;x16 clk, 1 stopbit,no parity, write reg 1
        DB      00H,03H         ;no interrupts, write reg 3
        DB      0E1H,05H        ;rx 8 bits, autoenables, rx enable,
                                ;write reg 5
        DB      0EAH            ;tx 8 bits, tx enable
CHANAE  EQU     $               ;end of table marker
;
CHANB:  DB      18H,04H
        DB      4CH,01H
        DB      00H,03H
        DB      0E1H,05H
        DB      0EAH
CHANBE  EQU     $               ;end of table marker
```

Channel A and B Baud Rate Software Example

After the SIO has been initialized, you should next set the Baud Rate for each of the two ports to match the device to which it is attached. Below is an example of setting the timer channel for each of the serial ports. Timer channel 0 controls serial port A, and Timer channel 1 controls serial port B. The crystal frequency used to

control the timer is a 2.4576 MHz crystal. This value lends itself to even binary divisions as illustrated below and can be used to program the timer channel directly as the count.

```
;
;equates for timer channel
;
TCH0    EQU     0B0H            ;channel 0 timer
TCH1    EQU     0B1H            ;channel 1 timer
TCMND   EQU     0B3H            ;timer command port
CHAMD   EQU     36H             ;chan 0 mode
CHBMD   EQU     76H             ;chan 1 mode
;
;baud rate equates
;
CLK     EQU     24576           ;crystal freq (KHz)
B38400  EQU     CLK/384/16      ;38,400 baud
B19200  EQU     CLK/192/16      ;19,200 baud
B9600   EQU     CLK/96/16       ;9600 baud
B4800   EQU     CLK/48/16       ;4800 baud
B2400   EQU     CLK/24/16       ;2400 baud
B1200   EQU     CLK/12/16       ;1200 baud
B600    EQU     CLK/6/16        ;600 baud
B300    EQU     CLK/3/16        ;300 baud
;
;set chan A baud rate subroutine
;
BAUDA:  LXI     D,B9600         ;select 9600 baud
        MVI     C,TCH0          ;reg c = timer chan 0 port
        MVI     A,CHAMD         ;get command byte
        OUT     TCMND           ;send to timer command port
        OUTP    E               ;send low baud byte
        OUTP    D               ;send high baud byte
        RET                     ;return to caller
;
;set chan B baud rate subroutine
;
BAUDB:  LXI     D,B19200        ;select 19200 baud
        MVI     C,TCH1          ;reg c = timer chan 1 port
        MVI     A,CHBMD         ;get command byte
        OUT     TCMND           ;send to timer command port
        OUTP    E               ;send low baud byte
        OUTP    D               ;send high baud byte
        RET                     ;return to caller
```

PERSONALITY BOARD - RS232/NO MODEM

PART NUMBER - RPB100

FUNCTION

The RS232/NO MODEM Personality Board provides RS232 drivers and receivers, terminations and jumper options to interface any simple RS232 device such as CRT terminals, serial printers or any other serial device not requiring an extensive handshake protocol, with the CPZ-48000 CPU.

INTERFACE REQUIREMENTS

CPU (J1)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSR*	DATA SET READY TO CPU
2	N/C	N/C
3	N/C	N/C
4	TxD	TRANSMIT DATA FROM CPU
5	RxD	RECEIVE DATA TO CPU
6	RTS*	REQUEST TO SEND DATA FROM CPU
7	CTS*	CLEAR TO SEND TO CPU
8	DCD*	DATA CARRIER DETECT TO CPU
9	DTR*	DATA TERMINAL READY FROM CPU
10	RNG*	RINGING INDICATOR TO CPU
11	N/C	N/C
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	N/C	N/C

PERIPHERAL (J2)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	SAFETY GND	SAFETY GROUND
2	TXD	TRANSMIT DATA FROM PERIPHERAL
3	RXD	RECEIVE DATA FROM PERIPHERAL
4	N/C	N/C
5	CTS*	CLEAR TO SEND TO PERIPHERAL
6	DSR*	DATA SET READY TO PERIPHERAL
7	POWER GND	POWER GROUND
8	DCD*	DATA CARRIER DETECT TO PERIPHERAL
9	N/C	N/C
10	N/C	N/C
11	N/C	N/C
12	N/C	N/C
13	N/C	N/C
14	N/C	N/C
15	N/C	N/C
16	N/C	N/C
17	N/C	N/C
18	N/C	N/C
19	SRTS*	SECONDARY REQUEST TO SEND FROM PERIPHERAL
20	DTR*	DATA TERMINAL READY FROM PERIPHERAL
21	N/C	N/C
22	N/C	N/C
23	N/C	N/C
24	N/C	N/C
25	N/C	N/C

CONNECTOR REQUIREMENTS

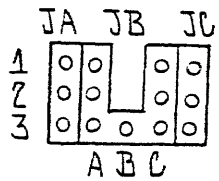
PERSONALITY BOARD CONNECTORS	MATING CONNECTORS
CPU - ANSLEY 609-1617	ANSLEY 609-1630 (ICM SUPPLIED)
Peripheral - CANNON DB25P-731	CANNON DB 25S-731 (CUSTOMER SUPPLIED)

SET UP INSTRUCTIONS

3 Jumper Areas are provided: JA , JB & JC

JA

The CPU may be required to provide handshaking with the peripheral through the signal " DCD". If that handshaking signal is required, connect pin 2 to pin 3 with the jumper provided. If no handshaking signal is required , connect pin 2 to pin 1.



JB

The CPU may required to provide handshaking with the peripheral through the signal "CTS". Furthermore, it may accept the signals "DTR" or "SRTS" through the input "CTS". The following options are available:

JB	Configuration
1a-2a	no handshaking provided to peripheral at "CTS"
2a-3a	peripheral's "CTS" activated by CPU's "DTR"
3a-3b	Not Used
3b-3c	no handshaking provided to CPU's "CTS" by peripheral's "DTR" or "SRTS"
2c-3c	peripheral's "DTR" or "SRTS" activates CPU's "CTS"
1c-2c	peripheral's "DTR" or "SRTS" activates CPU's "DSR"

JC

The peripheral may provide either of two handshaking signals "SRTS" or "DTR". This jumper may select either signal as the source to the CPU's "CTS" or "DSR" inputs.

EXAMPLES

1) Configure JA, JB and JC as follows for a single terminal interface:

JA = 1-2
JB = 1a-2a / 3b-3c / 2c-1c
JC=2-3

2) Configure JA, JB and JC as follows for an Anadex Serial Printer, model DP-9501

JA = 2-3
JB = 2a-3a / 2c-3c / 1c-2c
JC = 1-2

PERSONALITY BOARD - FLOPPY DISK CONTROLLER

PART NUMBER - FPB100-XY

FUNCTION

The FLOPPY DISK CONTROLLER personality board provides line drivers and receivers, terminators, logic and a jumper option to interface either an 8-inch or a 5 1/4-inch floppy disk drive with the CPZ-4800C CPU. A DB25 connector is available as the means to interface with the active interface; however, if the cable requires other types of commonly used connectors, adapters are available to tailor the interface appropriately.

INTERFACE REQUIREMENTS

CPU (J1)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	DS1*	DRIVE SELECT #1 FROM CPU
3	GND	GROUND
4	DS2*	DRIVE SELECT #2 FROM CPU
5	GND	GROUND
6	DS3*	DRIVE SELECT #3 FROM CPU
7	GND	GROUND
8	DS4*	DRIVE SELECT #4 FROM CPU
9	GND	GROUND
10	DIRC	DIRECTION CONTROL FROM CPU
11	GND	GROUND
12	STEP	STEP CONTROL FROM CPU
13	GND	GROUND
14	WRITE DATA	WRITE DATA FROM CPU
15	GND	GROUND
16	WGATE	WRITE GATE FROM CPU
17	GND	GROUND
18	TRACK 0*	TRACK 0 STATUS TO CPU
19	GND	GROUND
20	WRITE PROT*	WRITE PROTECT TO CPU
21	GND	GROUND
22	READ DATA*	READ DATA TO CPU
23	GND	GROUND
24	SSO	SIDE SELECT OUTPUT FROM CPU
25	GND	GROUND
26	HLD	HEAD LOAD COMMAND FROM CPU
27	GND	GROUND

28	INDEX*	INDEX PULSE TO CPU
29	GND	GROUND
30	READY	READY STATUS TO CPU
31	GND	GROUND
32	MOTOR ON	MOTOR ON STATUS FROM CPU
33	GND	GROUND
34	TK43	TRACK 43 STATUS FROM CPU
35	GND	GROUND
36	+16VDC	+16VDC
37	GND	GROUND
38	N/C	N/C
39	GND	GROUND
40	+5VDC	+5VDC

DB25 DRIVE INTERFACE (J2)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DS1*	DRIVE SELECT #1 to DRIVE interface
2	DS2*	DRIVE SELECT #2 to DRIVE interface
3	DS3*	DRIVE SELECT #3 to DRIVE interface
4	DS4*	DRIVE SELECT #4 to DRIVE interface
5	DIRC*	DIRECTION CONTROL to DRIVE interface
6	STEP*	STEP CONTROL to DRIVE interface
7	WRITE DATA*	WRITE DATA to DRIVE interface
8	WRITE GATE*	WRITE GATE to DRIVE interface
9	TRACK 0 *	TRACK 0 STATUS from DRIVE interface
10	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
11	READ DATA*	READ DATA to DRIVE inerface
12	SSO*	SIDE SELECT OUTPUT to DRIVE interface
13	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
14	INDEX*	INDEX PULSES from DRIVE interface
15	READY	READY STATUS from DRIVE interface
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	TK43*	TRACK 43 STATUS to DRIVE interface
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

8-INCH ADAPTER DRIVE INTERFACE (J-8IN)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	TK43*	TRACK 43 STATUS to DRIVE interface
3	GND	GROUND
4	N/C	N/C
5	GND	GROUND
6	N/C	N/C
7	GND	GND
8	N/C	N/C
9	GND	GROUND
10	N/C	N/C
11	GND	GROUND
12	N/C	N/C
13	GND	GROUND
14	SSO	SIDE SELECT OUTPUT to DRIVE interface
15	GND	GROUND
16	N/C	N/C
17	GND	GROUND
18	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
19	GND	GROUND
20	INDEX*	INDEX PULSES from DRIVE interface
21	GND	GROUND
22	READY*	READY STATUS from DRIVE interface
23	GND	GROUND
24	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
25	GND	GROUND
26	DS1*	DRIVE SELECT #1 to DRIVE interface
27	GND	GROUND
28	DS2*	DRIVE SELECT #2 to DRIVE interface
29	GND	GROUND
30	DS3*	DRIVE SELECT #3 to DRIVE interface
31	GND	GROUND
32	DS4*	DRIVE SELECT #4 to DRIVE interface
33	GND	GROUND
34	DIRC*	DIRECTION CONTROL to DRIVE interface
35	GND	GROUND
36	STEP*	STEP COMMAND to DRIVE interface
37	GND	GROUND
38	WRITE DATA*	WRITE DATA to DRIVE interface
39	GND	GROUND
40	WRITE GATE*	WRITE GATE to DRIVE interface
41	GND	GROUND
42	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
43	GND	GROUND
44	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
45	GND	GROUND
46	READ DATA*	READ DATA to DRIVE interface
47	GND	GROUND
48	N/C	N/C
49	GND	GROUND
50	N/C	N/C

5 1/4-INCH ADAPTER DRIVE INTERFACE (J-5 1/4IN)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	N/C	N/C
3	GND	GROUND
4	N/C	N/C
5	GND	GROUND
6	DS4*	DRIVE SELECT #4 to DRIVE interface
7	GND	GROUND
8	INDEX*	INDEX* PULSE STATUS from DRIVE interface
9	GND	GROUND
10	DS1*	DRIVE SELECT #1 to DRIVE interface
11	GND	GROUND
12	DS2*	DRIVE SELECT #2 to DRIVE interface
13	GND	GROUND
14	DS3*	DRIVE SELECT #3 to DRIVE interface
15	GND	GROUND
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	GND	GROUND
18	DIRC*	DIRECTION CONTROL to DRIVE interface
19	GND	GROUND
20	STEP*	STEP COMMAND to DRIVE interface
21	GND	GROUND
22	WRITE DATA*	WRITE DATA to DRIVE interface
23	GND	GROUND
24	WRITE GATE*	WRITE GATE to DRIVE interface
25	GND	GROUND
26	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
27	GND	GROUND
28	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
29	GND	GROUND
30	READ DATA*	READ DATA to DRIVE interface
31	GND	GROUND
32	SSO*	SIDE SELECT OUTPUT to DRIVE interface
33	GND	GROUND
34	N/C	N/C

MATING CONNECTOR REQUIREMENTS

Use the following table to determine the type of mating connector to use:

CONFIGURATION	PART NUMBER	CONNECTOR TYPE
8-INCH/HEADER PLUG ADAPTER	FPB100-11	ANSLEY 609-5030
8-INCH/EDGE CONNECTOR ADAPTER	FPB100-12	AMP 840-225F-A50-1
5 1/4-INCH/HEADER PLUG ADAPTER	FPB100-21	ANSLEY 609-3430
5 1/4-INCH/EDGE CONNECTOR ADAPTER	FPB100-22	AMP 840-225F-A34-1
8-INCH OR 5 1/4-INCH W/O ADAPTER	FPB100-00	CANNON DB25S-731

NOTE: MATING CONNECTORS ARE CUSTOMER SUPPLIED and the connector required is a function of the cable type the customer wishes to install. Connector equivalents may be used.

SET UP INSTRUCTIONS

Jumper PJA is provided to configure the base personality board for either 8-inch or 5 1/4-inch operation. The jumper selects the "READY" signal from the 8-inch drive interface or a signal generated on the basis of index pulse occurrances for the 5 1/4-inch drive operation. Install a jumper from pin 2 to 3 for 8-inch operation. Install a jumper from pin 1 to 2 for 5 1/4-inch operation.

(PJA)

PERSONALITY BOARD - RS232/FULL MODEM

PART NUMBER - MPB100

FUNCTION

The RS232C/FULL MODEM PERSONALITY BOARD provides RS232 drivers /receivers and jumper options to interface asynchronous or synchronous modems with varying types of bit oriented protocols such as IBM B. Sync, HDLC or SDLC. Jumpers provided enable the user to configure the board for either asynchronous or synchronous operation. If synchronous operation is selected, jumpers are provided to select either a baud rate clock or a transmit clock modem. In synchronous modems, the receive clock is always provided by the modem.

INTERFACE REQUIREMENTS

CPU (J1)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSR*	DATA SET READY TO CPU
2	N/C	N/C
3	N/C	N/C
4	TXD	TRANSMIT DATA FROM CPU
5	RXD	RECEIVE DATA TO CPU
6	RTS*	REQUEST-TO-SEND FROM CPU
7	CTS*	CLEAR-TO-SEND TO CPU
8	DCD*	DATA CARRIER DETECT TO CPU
9	DTR*	DATA TERMINAL READY FROM CPU
10	RNG*	RINGING INDICATOR TO CPU
11	N/C	N/C
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	N/C	N/C

PERIPHERAL (J2)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	SAFETY GND	SAFETY GROUND
2	TXD	TRANSMIT DATA TO PERIPHERAL
3	RXD*	RECEIVE DATA FROM PERIPHERAL
4	RTS	REQUEST-TO-SEND TO PERIPHERAL
5	CTS	CLEAR-TO-SEND FROM PERIPHERAL
6	DSR	DATA SET READY FROM PERIPHERAL
7	POWER GND	POWER GROUND
8	DCD	DATA CARRIER DETECT FROM PERIPHERAL
9	N/C	N/C
10	N/C	N/C
11	N/C	N/C
12	N/C	N/C
13	N/C	N/C
14	N/C	N/C
15	TXCLK	TRANSMIT CLOCK TO PERIPHERAL
16	N/C	N/C
17	RXCLK	RECEIVE CLOCK FROM PERIPHERAL
18	N/C	N/C
19	N/C	N/C
20	DTR	DATA TERMINAL READY TO PERIPHERAL
21	N/C	N/C
22	RNG	RINGING INDICATOR FROM PERIPHERAL
23	N/C	N/C
24	BAUD CLK	BAUD CLOCK TO PERIPHERAL
25	N/C	N/C

MATING CONNECTOR REQUIREMENTS

CUSTOMER TO SUPPLY

CANNON DB25S-731 or equivalent.

SET UP INSTRUCTIONS

The board may be configured for either asynchronous or synchronous modem requirements.

a) Asynchronous Modems

PJB, PJC, PJD, and PJE are all open.

b) Synchronous Modems

1) CPZ-48000 SUPPLIES TRANSMIT CLOCK

PJD, PJE, and PJC connected

Note: Cut PJB 1-2 and 2-3 on CPZ-48000 if using Port A of SIO.

Cut PJA on CPZ-48000 if using Port B of SIO.

2) CPZ-48000 SUPPLIES BAUD RATE CLOCK

Same as (1) above except PJB is connected instead of PJC.

c) If safety ground of the modem is to be tied to logic ground, connect PJA.